SERN. 7378

Digital Compact Cassette system DCC

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Basics of DCC
Integrated circuits for PASC
Circuit desription 70DCC300/70DCC380
Circuit diagram 70DCC300/70DCC380

DIGITAL dcc COMPACT CASSETTE

System description

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1. INTRODUCTION

The Digital Compact Cassette (DCC) is the logical successor to the Compact Cassette (CC), which was introduced in 1963 by Philips and has since developed into an extremely successful sound carrier. The secret of the success of the Compact Cassette is the unique versatility of the system, which has found applications not only in devices used at home, but also in the car hi-fi and portable audio field. In spite of numerous improvements of quality, both mechanical and electronic, as well as noise suppression techniques like Dolby B/C, even the most expensive cassette decks do not reach the high standard of CD sound. What was wanted was a digital recording medium which would offer the ease of operation of digital media as well as high dynamic range and minimum noise. R-DAT ("Rotary head Digital Audio Tape") was therefore introduced internationally in 1982, and S-DAT ("Stationary head Digital Audio Tape") in 1985.

While R-DAT found a foothold mainly in the semi-professional field, it was a commercial failure in the entertainment electronics sector. The likely reasons are the high purchase price because of the complex mechanics, and the poor range of pre-recorded tapes on offer.

S-DAT used a new head technology (magneto-resistive, integrable thin film heads), the production of which caused considerable problems, because of the high data rates and the associated high number of tracks (20 for the low frequency signal, with the same tape speed and identical dimensions as for CC).

However, the decisive disadvantage of both systems is without any doubt the lack of "backwards compatibility" with CC, which is by far the most commonly used sound carrier (about 2.600.000.000 blank and recorded cassettes and 180.000.000 cassette recorders and players were sold last year alone). The enormous potential of existing CCs (about 60 tapes per household) could not be ignored, so it had to be possible to continue to use traditional cassettes. Philips has met these requirements with the DCC system.

DCC is an S-DAT system, which has only become possible in the 90s, by use of new technologies in the sound head and a clever method of data reduction.

2.1. THE DIGITAL COMPACT CASSETTE

To ensure that the DCC is backwards compatible with the Compact Cassette, it has almost the same external dimensions. However, it is only 9,6mm thick, compared to 12mm for the CC.
On the other hand, there are some technical differences:

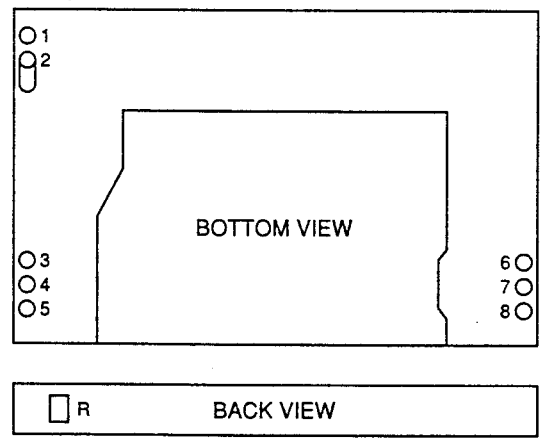
- The tape material used is CrO_2, which is also used for video tapes. The width of the tape is defined as 3,78mm (0,01mm), so the tolerance is less than that of the CC (+0,03/-0,02mm). On this 3,78mm, DCC cassettes have altogether 2 x 9 parallel data tracks, each with a width of 185µm, and with a 10m separation between them. The separation between track 7 on side A and track 7 on side B is 95µm wide. Track 0 begins 97,5µm from the edge of the tape.

- A slider protects the free parts of the tape from dust and contact, in a similar way to a 3 1/2" computer disk. Also, both tape spools are locked, so that the tape cannot unwind of its own accord. The well-known experience of the CC tape being "chewed up" by the machine is well and truly a thing of the past.

- Openings for the hubs are only provided on one side, since DCC devices are always equipped with auto-reverse drives. The top side therefore offers a large area to display the title, etc.

- The DCC has a recording protection switch on the bottom side of the cassette.

- A special hole code on the bottom side of the DCC enables the recorder to read information about tape thickness and length directly from blank cassettes.



For blank cassettes:
1 .....DCC/CC identifier; DCC = open, CC = closed
2 .....recording protection switch, mechanically connected to R
R.....recording protection for DCC and CC at back of cassette; protected = closed

3, 4, 5 .....tape length (for blank cassettes only)

	45	60	75	90	105	120	
3	O	C	O	C	O	C	
4	O	O	C	C	O	O	
5	O	O	O	O	C	C	O...open, C...closed

Hole 5 also indicates the tape thickness; 12µm (total playing time 90min) = open, 9µm (total playing time > 90min) = closed

6, 7, 8 .....reserved for future use

For pre-recorded tapes:
1 .....open
2 .....closed
R.....not present
3, 4, 5 .....closed
6, 7, 8 .....reserved for future use

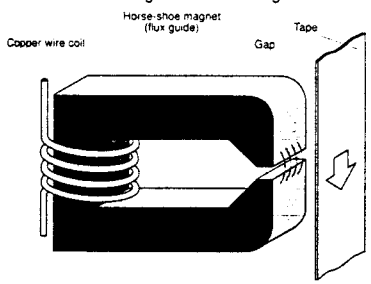
2.2. THE DCC HEAD

The system makes high demands on the DCC head (2 x 9 parallel digital tracks on a tape only 3,78mm wide), and these can no longer be met by wound coils. The combined recording and playback heads are therefore implemented in thin film technology.
Each DCC head consists of 3 functional units:
- 9 IRH head gaps (Inductive Recording Heads) for digital recording, each 185µm wide.
- 9 MRH head gaps (Magneto-Resistive Heads) for digital playback, each 70µm wide. The separation between two MRH head gaps is 10µm.
- 2 MRH head gaps for analog playback, each 600µm wide.

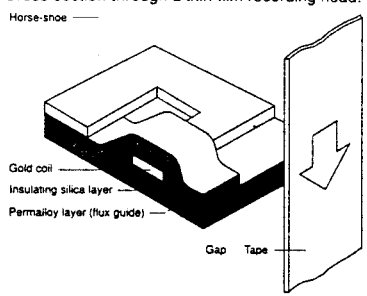
INDUCTIVE RECORDING HEAD "IRH"

The principle function of an IRH is identical to conventional CC-recording heads. The magnetic field produced by the write current is coupled into a flux guide and transferred onto the tape via a gap. DCC recording heads are produced by use of thin-film technology. Compared to a conventional CC-head there is only one coil (more turns would cause more layers, which are rather complicated to produce).

Cross section through a CC-recording head:



Cross section through a thin-film recording head:



Since the magnetic flux is $\Theta = I * N$, in case of the IRH with N=1 a high write current is necessary. This current is approximately 120..180mA per track with a pulse width of 300ns. Due to thermic reasons the heads are not writing simultaneously, but time delayed. In recording mode the tape is magnetized in two directions: "1" in tape transport direction, and "0" vice versa. The length of each single bit is 500nm.
The depth of magnetization is determinated by the write current. If the value of the current is too high, overwriting will be critical, else reading.

MAGNETO-RESISTIVE HEAD "MRH"

Conventional CC-reading heads act according to the inductive law. Changing magnetization of the moving tape inducts a certain voltage into the coil of the playback head. Different to that the DCC playback head uses a magneto-resistive principle.
The basic element of an MRH is a thin and narrow stripe, made of ferromagnetic polycristalline alloy (e.g. Permalloy: 80% Fe, 20% Ni). This thin layer is mounted on an isulating carrier (e.g. SO_2). The stripe is magnetized length wise by the spontaneous field M_S.
This orientation is achieved by a special production process ("sputtering"), where the stripe is exposed to a strong continuous magnetic field. Sputtering is a process to manufacture extremly thin layers. Strong external fields can cause a 180° shift of this spontaneous magnetization M_S, and destroy the head. For protection against above mentioned effect, a permanent magnetic field parallel to the spontaneous magnetization is used. This is realized by a small permanent magnet near by the stripe. The magnet causes a slight decrease of the sensitivity. However, the head is still sensitive against external fields. Therefore demagnetizing cassettes **must not** be used.
The field of the permanent magnet should not be mixed up with a bias field, which is inducted by a bias current perpendicular to the inner field (see next page).
The inducted magnetic field H from the tape causes a maximum phaseshift of 90° compared to the length wise magnetization. The resistance of the stripe will change to ±3%.

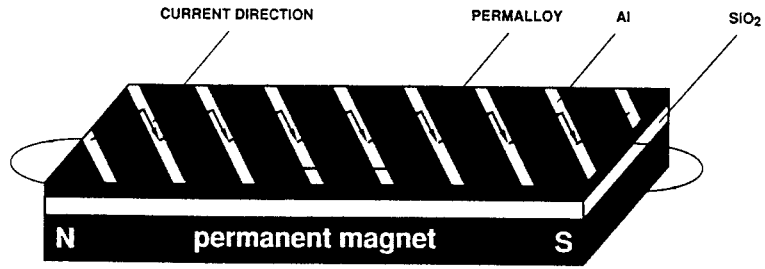
$$\rho(\Theta) = \rho 0 + \Delta\rho max * \cos^2 \Theta$$

Θ.....Angle of magnetization compared to the axis of the stripe
$\rho 0$.....Specific resistance of the stripe at $\Theta = \rho 0$
ρ_{max}...maximum change of the stripe resistance

Considering that the inducted field H from the tape is always perpendicular to the stripe axis and ignoring demagnetization and anisotropical fields leads to:

$$\rho(H) = \rho 0 + \Delta\rho_{max} * (1 - \frac{H^2}{M^2})$$

The magnetization of the stripe is aligned to the current flowing through the stripe by the internal magnetization M_i. Above formula is non-linear and has different meanings, because two counterphase external fields would cause equal change of resistance. According to this the stripe is not useful for detection of data, yet. Therefore additional, well conductive, parallel stripes (e.g. Al) are mounted onto the surface of the ferromagnetic basic layer on an angle of 45°. The resulting structure is called "barberpoles". Due to the much higher conductivity of Al the current-angle in the area of the barberpoles will become 45°. The current flow through the MRH will be in a zigzag course.

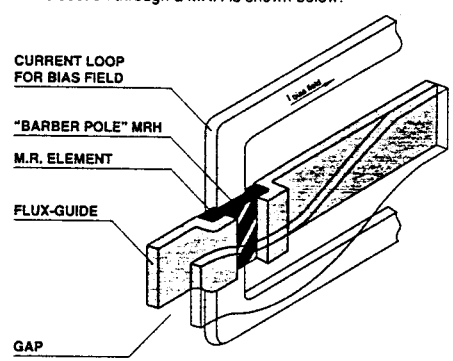


In above formula Θ can be replaced by Θ - 45°, what results in:

$$\rho = \rho 0 + \frac{\Delta\rho max}{2} + \Delta\rho_{max} * \frac{H}{M}\sqrt{1 - \frac{H^2}{M^2}}$$

It can be seen that the correlation between specific resistance and influencing field is approximately linear for small external fields.

A cross section through a MRH is shown below:

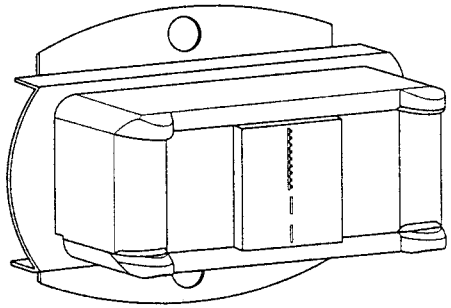


The magnetization of the tape is coupled into the magneto-resistive stripe via the flux guide. Due to the changing magnetization of the tape, the resistance of the MRH will also change. The bias field is fixed by a bias current of about 10mA. A small permanent magnet protects against demagnetization due to strong external fields.
If the MRH is supplied by a constant current source, the variable resistance will result in an alternating voltage:
$\Delta u = I_{const} * \Delta r(H)$
The current I_{const} is about 10mA, the resistance of a head about 100Ω. The alternating voltage, forced by the changing magnetization of the tape, will be about 50µVpp, what is rather small.

2.2.1. DCC HEAD VERSIONS

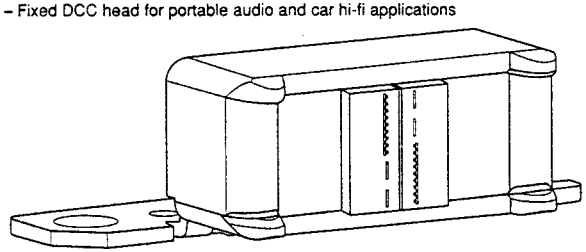
In principle, two DCC head versions are possible:

– DCC auto-reverse head



The nine digital and two analog head gaps are arranged one above the other, and each take up half the sound head height. By using the turning mechanism, the tape can be scanned in both directions in digital and analog fashion.

– Fixed DCC head for portable audio and car hi-fi applications

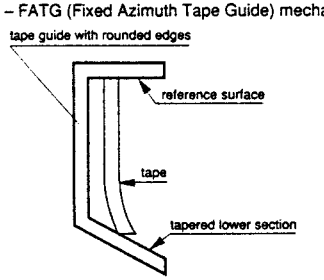


This head consists of two adjacent complete sound head units, turned through 180°. The turning mechanism, which takes up a lot of space, is therefore unnecessary.

2.2.2. TAPE GUIDANCE

Tape guidance for DCC devices is considerably more complex than for CC recorders. There are essentially two mechanisms for precise tape guidance and close tape-head contact:

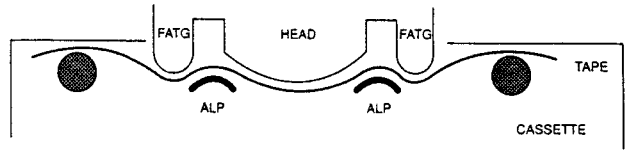
– FATG (Fixed Azimuth Tape Guide) mechanism



FATG shown for one side of the head

A pair of tape guidance pins is fitted to each end of the sound head. The lower pins are slanted, so that the tape is slightly curved as it passes. This stiffens the tape, so that it can be guided exactly to the azimuth reference line (the stop line of the upper peg). This mechanism, which is patented by Philips, effectively prevents azimuth faults.

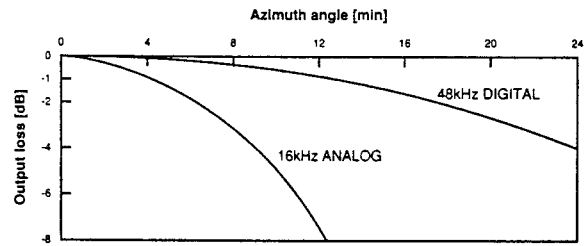
– ALPs (Azimuth Locking Pins)



Two ALPs are fitted to the DCC cassette, to press the tape into the fixed FATG mechanism. By this method, the contact area of the tape and the sound head is increased, and the tape-head contact is considerably improved.

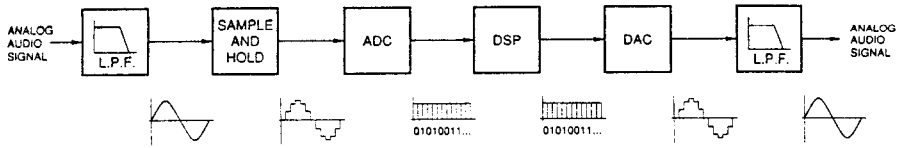
2.2.3. AZIMUTH

The DCC is considerably less sensitive to azimuth faults than the CC, in which even small angle errors cause great amplitude losses.



3. PRINCIPLES OF DIGITAL SIGNAL PROCESSING

DCC is a digital tape system for sound recording, in which audio signals are stored on tape in digital form. For this purpose, it is first necessary to digitize the analog music signal, i.e. to do an A/D conversion. The data is then extensively manipulated (DSP – Digital Signal Processing), and finally stored on the tape. For playback, after decoding (regaining the original digital audio data), there must be a D/A conversion. This can be shown schematically as follows:



Note: since the analog components before the ADC and after the DAC certainly do not improve the sound quality, attempts are made to keep them to a minimum.

3.1.INPUT LOW PASS FILTER (ANTI-ALIASING FILTER)

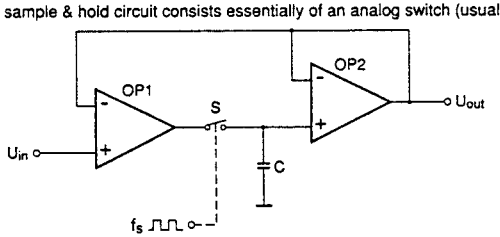
The low pass filter on the input side must ensure that the input signal to be scanned has no components with frequencies above half the scanning frequency. Failure to limit the bandwidth in this way causes aliasing distortions, which make it impossible to regain the original analog signal. (See 3.3. Principles of A/D conversion).

This places great demands on the anti-aliasing filter:
- it must be linear up to the upper limit frequency
- the transition between the pass range and the stop range must be steep
- low non-linear distortion factor and minimum self-generated noise
- low on and off transient effects
- low phase distortion.

At first sight, these requirements include mutually exclusive properties. Filters with steep edges often have strong phase distortion in the transition range, bad on and off transient effects and strong ripple. These effects can be overcome with carefully dimensioned, active filters, but they require complex circuits. A much more elegant solution is digital filtering combined with oversampling. This method is described in more detail in 3.3.1. Sigma-delta A/D converter.

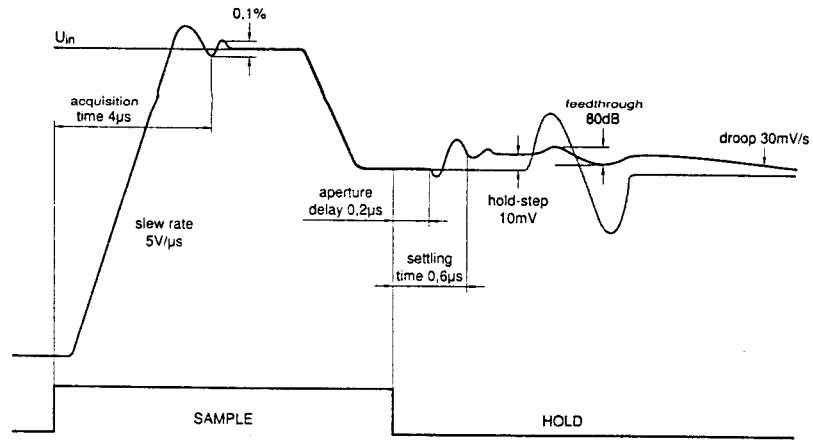
3.2. SAMPLE&HOLD CIRCUIT

A sample & hold circuit consists essentially of an analog switch (usually an FET), a storage capacitor and buffer stages.



If switch S is closed, capacitor C is charged to the momentary amplitude value of the input voltage. If S is opened, the voltage remains stored in C. The voltage at the circuit output can now be further processed, independently of subsequent changes of the input voltage. OP1 prevents loads on the voltage source, and must supply high currents to recharge C quickly. To keep the self-discharging current of C as low as possible, the capacitor must have good insulation (Teflon, polystyrene and polypropylene are suitable dielectrics). Also, switch S should have a high blocking resistance, and OP2 should have a high input resistance (FET input).

The typical faults of a real sample & hold circuit are shown in the diagram below.

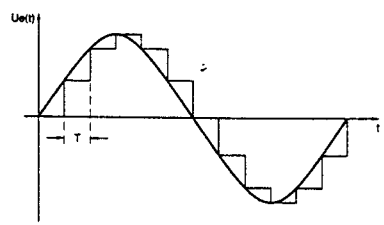


- After the switch is closed, the output voltage of OP1 does not immediately follow the value of the input voltage, but rises at a definite rate, the so-called "slew rate" of the operational amplifier. The time between closing the switch and reaching the correct output voltage is called "acquisition time".
- On transition to the hold state, there is a delay before the switch opens. This is called "aperture delay", and often varies according to the input voltage ("aperture jitter").
- Because of the capacitance of the switch, when it is opened a small charge is coupled to the storage capacitor. The result is usually a voltage jump followed by a transient effect ("hold-step").
- Because of the capacitive voltage divider formed by the capacitance of the switch and the storage capacitor, part of the input voltage affects the output ("feedthrough").
- The input current of OP2 and the blocking current of the switch further discharge the storage capacitor. This effect is called "droop".

The quality of the sample & hold circuit is mainly determined by acquisition time and droop. For audio applications, the circuit is usually implemented in the ADC, and the storage capacitor is usually attached externally. In this way, it can be adapted to the required application (within limits).

3.3. PRINCIPLES OF A/D CONVERSION

Assume an arbitrary input signal f(t).

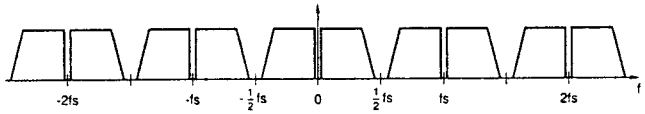


This input signal is sampled at intervals of T, i.e. the signal form is scanned. T is called the scanning time, and the scanning (or sampling) frequency fs is defined as 1/T. It can be seen that the higher fs is, the less the resulting step function differs from the input signal. The lowest scanning frequency at which the analog input signal can still be correctly reconstructed is given by Shannon's scanning theorem:

" Any continuous signal is completely characterised by the sequence of its scanning values if the scanning frequency is greater than twice the highest frequency in the signal ".

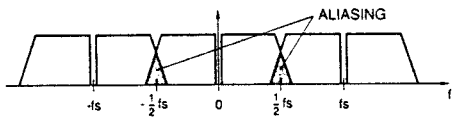
The scanning theorem can be represented clearly in the frequency domain. An idealised frequency response of an audio signal, which is ideally flat in the frequency range 20Hz..20kHz and falls steeply outside it, is assumed.

By Fourier transform, it is shown that the spectrum of the input signal after scanning looks like this:

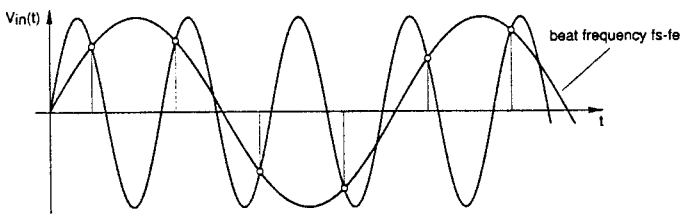


The diagram shows that the spectrum of the scanned signal repeats periodically with the sampling frequency fs.

If the scanning frequency is less than it should be according to the scanning theorem, parts of the spectrum appear with the difference frequency (fs - f) < fmax, and result in beating (aliasing) in the output signal.



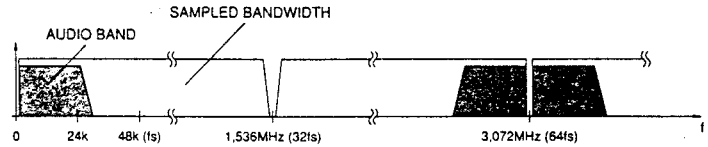
It can be seen that, because of the intersection of the spectra, these parts of the spectrum of the input signal are not simply lost, but reflected inversely into the effective range, so that the original signal can no longer be uniquely reconstructed.



3.3.1. SIGMA-DELTA A/D CONVERTER

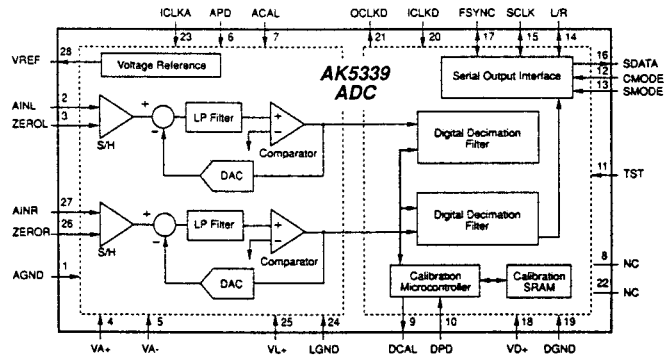
The characteristic of the sigma-delta A/D converter is the 1-bit conversion principle with 64-fold oversampling. This technique reduces the number of analog components to a minimum, so that the problems with external anti-aliasing filters and reference current sources, etc. are eliminated.

The converter scans the audio signal at 64 times the nominal sampling frequency (32kHz, 44,1kHz or 48kHz). This collects all frequencies included in the audio signal up to 1,53MHz (if fs = 48kHz).



The frequencies between 20kHz and 1,53MHz, which are actually unnecessary, are eliminated in the ADC by a high-order digital anti-aliasing filter with high blocking attenuation. The scanning rate is then reduced to its nominal value, i.e it is "down-sampled" or "decimated". The integrated digital filter is an FIR (finite impulse response) filter with linear phase in the pass range, so that phase distortions do not occur. For the external input filter, an analog low pass filter with a limit frequency in the MHz range is enough to suppress the spectral components at 64fs = 3,072MHz.

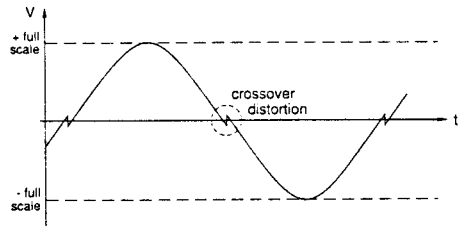
BLOCK DIAGRAM AND PIN CONFIGURATION OF A SIGMA-DELTA ADC (e.g. the Crystal AK5339):



1	AGND	analog ground (0V)
2	AINL	analog input left
3	ZEROL	zero input left
4	VA+	positive supply voltage (+5V) analog
5	VA-	negative supply voltage (-5V) analog
6	APD	analog power down input
7	ACAL	analog calibrate input
8	n.c.	not connected
9	DCAL	digital calibrate output
10	DPD	digital power down input
11	TST	test input
12	CMODE	clock mode selection
13	SMODE	serial I/O mode selection
14	L/R	left/right selection
15	SCLK	serial data clock
16	SDATA	serial data output
17	FSYNC	frame sync signal
18	VD+	positive supply voltage (+5V) for the digital section
19	DGND	digital ground (0V)
20	ICLKD	clock input for the digital section
21	OCLKD	clock output for the digital section
22	n.c.	not connected
23	ICLKA	clock input for the analog section
24	LGND	ground (0V) for logic in the analog section
25	VL+	positive supply voltage (+5V) for logic in the analog section
26	ZEROR	zero input right
27	AINR	analog input right
28	Vref	voltage reference output

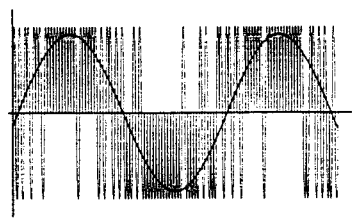
3.4. BITSTREAM D/A CONVERTER

Digital/analog conversion is one of the most critical parts of digital audio equipment.
A traditional 16-bit DAC creates the output signal from 16 different current sources, which differ from each other by a factor of 2. In this way, a total of $2^{16} = 65536$ different signal levels can be output. The exactness of these signal sources is decisive for the quality of the converter. For a 16-bit DAC, the current for the MSB (most significant bit) must be exactly $2^{15} = 32768$ times the current for the LSB (least significant bit). Every deviation of a current source from its desired value causes non-linearities, which are particularly disturbing at low output levels.
Another source of errors is asynchronous switching on and off of the current sources. These distortions are also called "glitches".



Although exact equalisation of the current sources by laser (laser trimming), or additional deglitcher circuits, can reduce these distortions, problems of long-term drift of the component values (ageing) remain.

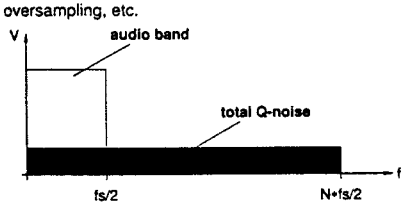
In 1989, Philips therefore presented an entirely new concept – the "bit stream" DAC.
In this converter, the 16 switches of traditional multi-bit DACs are replaced by one switch. This means that instead of 65536 different output levels only two logical states, "on" and "off", exist. So that each of the 65536 required levels can still be represented, the switching frequency is increased to many times the sampling frequency (e.g. 256fs for the SAA7323). Each output level is then represented by a particular bit pattern (a sequence of "0"s and "1"s).



For example, digital zero (digital silence) is represented by the bit pattern 1010..., which (averaged over time) corresponds exactly to the value 0,5. Signal levels greater than zero therefore include more 1s than 0s, and vice versa for levels less than zero.

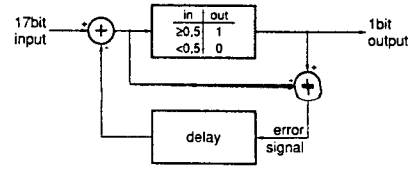
3.4.1.NOISE SHAPING

The signal-to-noise ratio of a DAC is 6dB per bit. A 16-bit system therefore has an SNR of 16 x 6dB + 2dB = 98dB.
The SNR of a 1 bit converter is therefore only 8dB. By oversampling, the effective noise power is distributed over a broader frequency spectrum. This reduces the SNR in the audio range by 3dB for two-fold oversampling, by 6dB for four-fold oversampling, etc.



For 256-fold (2^8) oversampling, it follows that SNR = 8 x 3dB + 8dB = 32dB.
For quality audio applications, this value is evidently unsatisfactory or worse. With the bit stream, an additional digital circuit called the "noise shaper" is therefore used. In this technique, the quantisation error is coupled back to the input, so that the quantisation noise is shifted out of the audio range into higher frequencies.

The method of operation of a noise shaper can be represented by the following block diagram:



Example: output signal 0,5 (digital silence)

input	output	error signal feedback
0,5	1	0,5
0,5 - 0,5 = 0	0	0
0,5 - 0 = 0,5	1	0,5
0,5 - 0,5 = 0	0	0

In this case the "bit stream" 1010..., which (averaged) corresponds exactly to the required value 0,5, is produced.

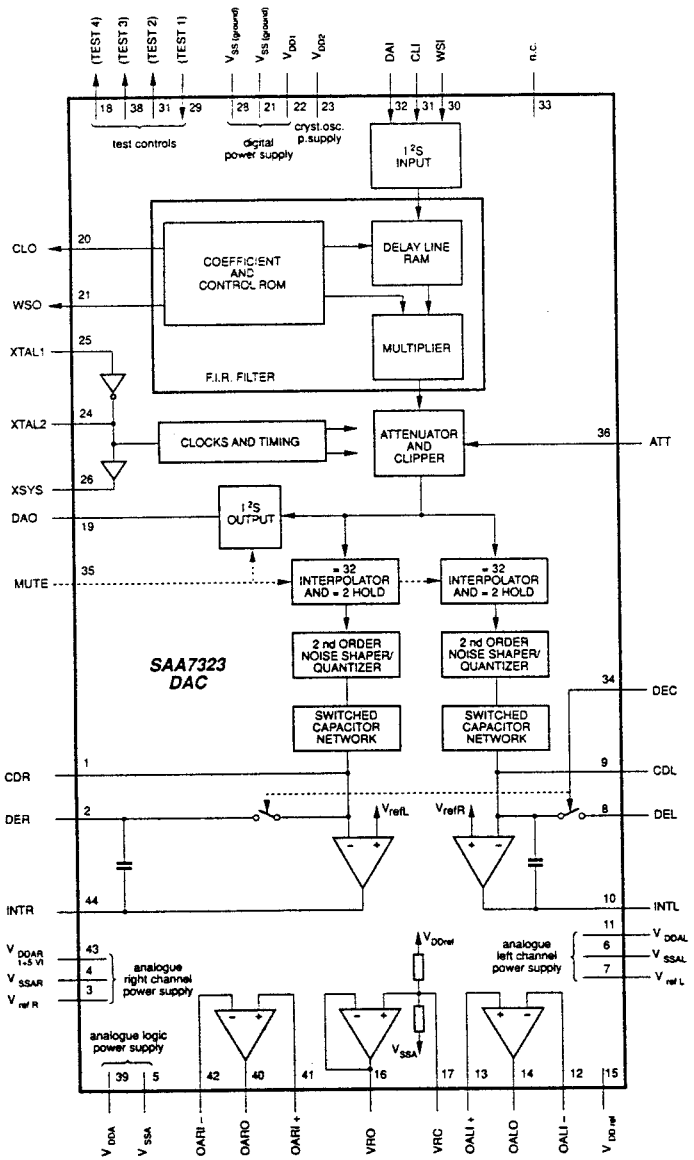
Example: output signal 0,8

input	output	error signal feedback
0,8	1	0,2
0,8 - 0,2 = 0,6	1	0,4
0,8 - 0,4 = 0,4	0	-0,4
0,8 + 0,4 = 1,2	1	-0,2
0,8 + 0,2 = 1	1	0

In this case the "bit stream" 11011..., which (averaged) corresponds to the required value 0,8, is produced.

The two examples involve constant input signals. Of course, the method can also be used for musical signals. The output signal of the noise shaper is taken directly to the 1 bit DAC, which is implemented as a switchable capacitor. In practice, higher order noise shapers are used, which make even more efficient noise transformation possible.

BLOCK DIAGRAM AND PIN CONFIGURATION OF BIT STREAM DAC SAA7323 (with second-order noise shaper):



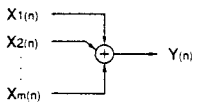
1	CDR	capacitor damping right
2	DER	de-emphasis right
3	VrefR	reference voltage input right for the analog channel ground (normally connected to VRO)
4	VssAR	ground connection for the analog right channel
5	VssA	ground connection for logic in the analog section
6	VssAL	ground connection for the analog left channel
7	VrefL	reference voltage input left for the analog channel ground (normally connected to VRO)
8	DEL	de-emphasis left
9	CDL	capacitor damping left
10	INTL	integrator output left
11	VDDAL	positive supply voltage (+5V) for the analog left channel
12	OALI-	operational amplifier left input -
13	OALI+	operational amplifier left input +
14	OALO	operational amplifier left output
15	VDDref	positive supply voltage (+5V) for the reference voltage generator
16	VRO	reference voltage output (+2,5V typ.)
17	VRC	reference voltage capacitor
18	TEST4	test output 4 (do not connect)
19	DAO	I²S-serial data output
20	CLO	I²S-serial bit clock output (5,6448MHz typ.)
21	WSO	I²S-word select output (176,4kHz typ.)
22	VDD1	positive supply voltage (+5V) for the digital section
23	VDD2	positive supply voltage (+5V) for the crystal oscillator
24	XTAL2	crystal oscillator output
25	XTAL1	crystal oscillator input
26	XSYS	system clock output
27	Vss	supply ground (0V)
28	Vss	supply ground (0V)
29	TEST1	test output 1 (connected to ground)
30	WSI	I²S-word select input
31	CLI	I²S-serial bit clock input
32	DAI	I²S-serial data input
33	n.c.	not connected
34	DEC	de-emphasis control
35	MUTE	mute (actice low)
36	ATT	attenuation (when active low this control input provides -12dB attenuation to the analog output)
37	TEST2	test output 2 (do not connect)
38	TEST3	test output 3 (do not connect)
39	VDDA	positive supply voltage (+5V) for logic in the analog section
40	OARO	operational amplifier right output
41	OARI+	operational amplifier right input +
42	OARI-	operational amplifier right input -
43	VDDAR	positive supply voltage (+5V) for the analog right channel
44	INTR	integrator output right

3.5. PRINCIPLES OF DIGITAL FILTERS

In digital audio engineering, it is natural to implement filter functions in digital form, since the audio signals are already present in the form of quantised scanning values.

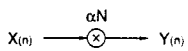
The three basic components of a digital filter are:

– Adder



$Y(n) = X1(n) + X2(n) + ... + Xm(n)$

– Multiplier



$Y(n) = \alpha N * X(n)$

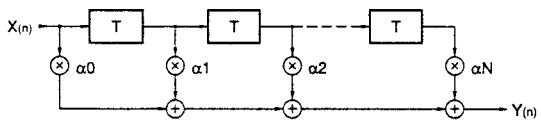
– Delay

$Y(n) = X(n-T)$

Digital filters are divided into two groups:

3.5.1. Finite Impulse Response Filter ("FIR filter")

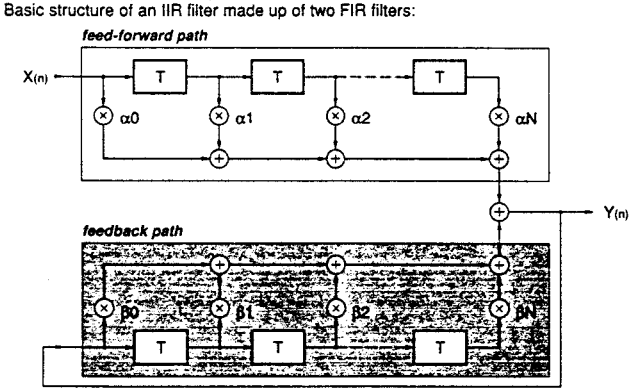
Basic structure of an FIR filter:



These filters have no back-coupling branch, and are therefore also called "non-recursive filters". Because there is no feedback, FIR filters are always stable, i.e. they have no tendency to oscillate.
The output signal of an FIR filter is the sum of a finite number of terms. Each term consists of the product of a (delayed) scanning value and a constant factor, the so-called filter coefficient. The number of terms determines the order of the filter.

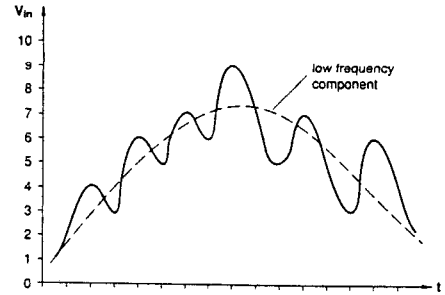
3.5.2. Infinite Impulse Response Filter ("IIR-Filter")

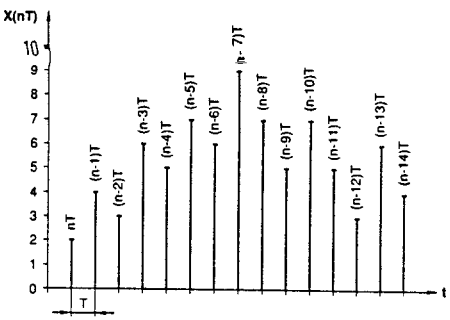
Basic structure of an IIR filter made up of two FIR filters:



In IIR filters, the output signal is not only determined by the input values, but previous output values are also fed back to the input. IIR filters therefore have a feedback branch, and are also called "recursive filters" because of their infinite step response. IIR filters are more difficult to control than FIR filters, not least because of their tendency to oscillate, and they are not as common in digital audio engineering.

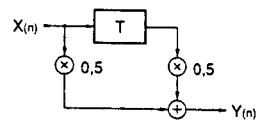
The operation of a digital filter can be explained by reference to a simple first-order low-pass filter.
A continuous signal which is converted into discrete form and digitized by means of sampling and A/D-conversion will have the appearance as follows:





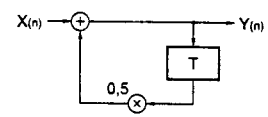
The figures below show the principal structure of the FIR- resp. IIR-filter and their differential equations:

– FIR-Filter



$Y(nT) = 0{,}5*X(nT) + 0{,}5*X(nT-T)$

– IIR-Filter

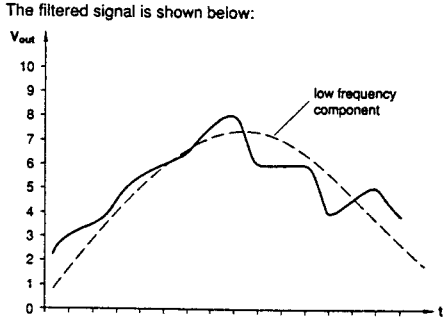


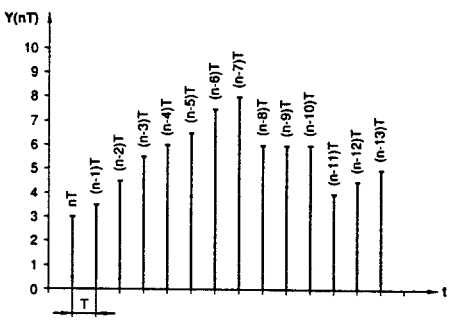
$Y(nT) = X(nT) + 0{,}5*X(nT-T)$

The calculations for the FIR-filter give following output values of the filtered samples:

Y(nT)	= 0,5*X(nT)	+ 0,5*X(nT-T)	= 0,5*2 + 0,5*4 = 3	Y(nT-7T)	= 0,5*X(nT-7T)	+ 0,5*X(nT-8T)	= 0,5*9 + 0,5*7 = 8
Y(nT-T)	= 0,5*X(nT-T)	+ 0,5*X(nT-2T)	= 0,5*4 + 0,5*3 = 3,5	Y(nT-8T)	= 0,5*X(nT-8T)	+ 0,5*X(nT-9T)	= 0,5*7 + 0,5*5 = 6
Y(nT-2T)	= 0,5*X(nT-2T)	+ 0,5*X(nT-3T)	= 0,5*3 + 0,5*6 = 4,5	Y(nT-9T)	= 0,5*X(nT-9T)	+ 0,5*X(nT-10T)	= 0,5*5 + 0,5*7 = 6
Y(nT-3T)	= 0,5*X(nT-3T)	+ 0,5*X(nT-4T)	= 0,5*6 + 0,5*5 = 5,5	Y(nT-10T)	= 0,5*X(nT-10T)	+ 0,5*X(nT-11T)	= 0,5*7 + 0,5*5 = 6
Y(nT-4T)	= 0,5*X(nT-4T)	+ 0,5*X(nT-5T)	= 0,5*5 + 0,5*7 = 6	Y(nT-11T)	= 0,5*X(nT-11T)	+ 0,5*X(nT-12T)	= 0,5*5 + 0,5*3 = 4
Y(nT-5T)	= 0,5*X(nT-5T)	+ 0,5*X(nT-6T)	= 0,5*7 + 0,5*6 = 6,5	Y(nT-12T)	= 0,5*X(nT-12T)	+ 0,5*X(nT-13T)	= 0,5*3 + 0,5*6 = 4,5
Y(nT-6T)	= 0,5*X(nT-6T)	+ 0,5*X(nT-7T)	= 0,5*6 + 0,5*9 = 7,5	Y(nT-13T)	= 0,5*X(nT-13T)	+ 0,5*X(nT-14T)	= 0,5*6 + 0,5*4 = 5

The filtered signal is shown below:





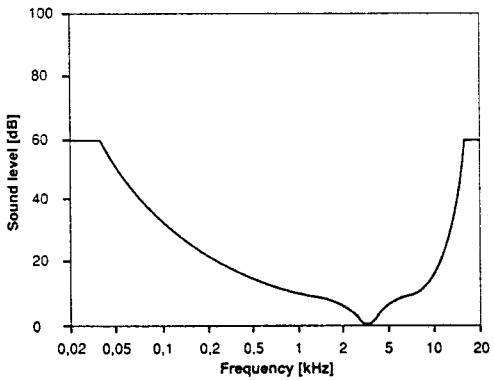
A number of higher-order components have been filtered-out, but the result is still not an ideal low-frequency signal. If the number of elements is increased to make a higher-order filter, the filtered signal will approximate the original low-frequency component. The calculations become much more extensive since more preceding samples need to be included.

4. PRINCIPLES OF PSYCHO-ACOUSTICS

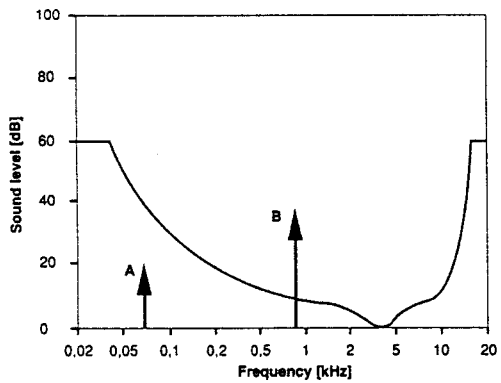
In all digital recording methods until now, the bit sequence from the output of the A/D converter was transferred unchanged to the recording medium (full format recording). In DCC, for the first time, an ingenious coding procedure is used, and makes possible an appreciable reduction of the data to be recorded, without any audible loss of quality. This is made possible by reducing redundancy, and by eliminating irrelevant parts of the signal, taking into account special psycho-acoustic effects.

4.1. THE HEARING THRESHOLD

The human ear is not equally sensitive to all audible frequencies, but has a "frequency response", the so-called hearing threshold:



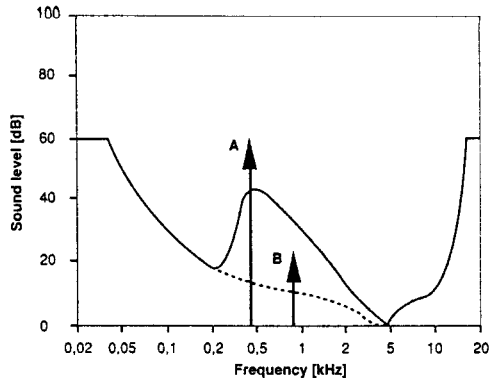
It can be seen that human hearing is most sensitive to frequencies in the range 2..5 kHz. To make a 20Hz or 20kHz sound audible requires about 10^6 times as much power as for a 3kHz sound, and in practice such sound levels will be rather rare. Signals which lie below the hearing threshold have no subjective effect on hearing, and therefore need not be coded or recorded.



In the example above, signal B is audible because its amplitude is over the hearing threshold. Signal A lies below the hearing threshold, so that it cannot be perceived, and is not recorded.

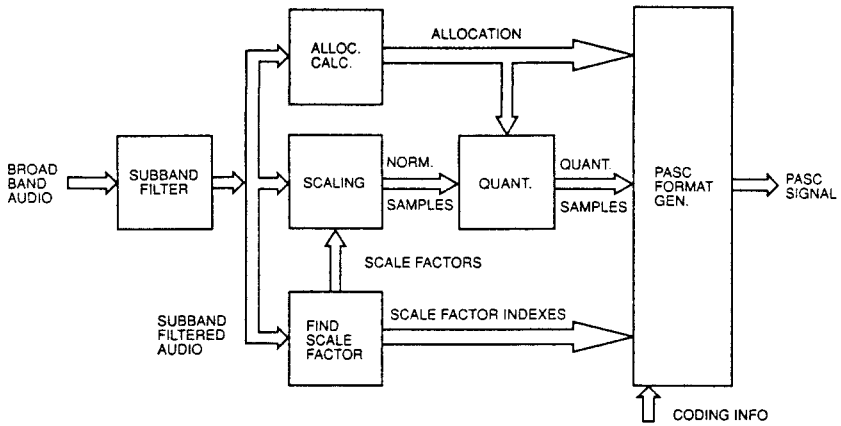
4.2. THE MASKING EFFECT

This effect occurs if there are components of the spectrum which are close together and have different amplitudes. A high power signal (A) causes the hearing threshold around it to be raised, so that neighbouring lower power signals, which by themselves would be audible (signal B), are masked.



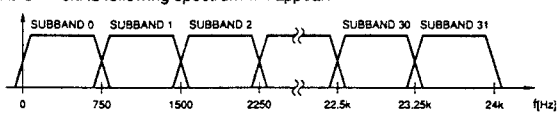
The psycho-acoustic effects described above concern the frequency domain. There are also effects in the time domain, but these are unimportant for the coding procedure used in the DCC system.

5. PASC (Precision Adaptive Subband Coding)



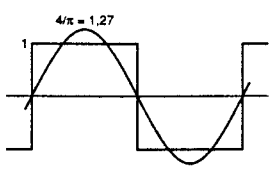
5.1. DECOMPOSITION OF A DIGITAL BROAD BAND SIGNAL INTO SUBBANDS

The audio signal supplied by the ADC or digital input is first divided into 32 subbands (in separate channels). One subband filter (SBF) is required for each channel. The bank of the SBF processes the input samples (maximum quantisation 18 bits) with an internal precision of 24 bits. The individual subbands have a bandwidth of fs/64.
At fs = 48kHz following spectrum will appear:



Given the bandwidth of fs/64, the scan rate per subband is reduced to fs/32 (down-sampling). For each input sample, 32 filtered samples (one for each subband) with a resolution of 24 bits are output, and the data rate per subband is reduced to 1/32 fs. The data rate of 18 bits x fs therefore becomes 32 x 24 bits x fs/32. Up to now, the data has not been reduced, but the quantisation has been raised from a maximum of 18 bits to 24 bits.

The 24-bit quantisation of the subband samples means that a dynamic range of +6 to -140dB is covered (SNR = 6dB x 24 bits + 2dB). The extension of the dynamic range is necessary because amplitudes above the maximum amplitude of the broad band signal can occur in a subband signal ("Gibbs phenomenon"). For instance, the fundamental wave of a square signal is above the amplitude of the actual square signal by a factor of $4/\pi$.



5.2. CALCULATION OF SIGNAL POWERS OF SUBBANDS

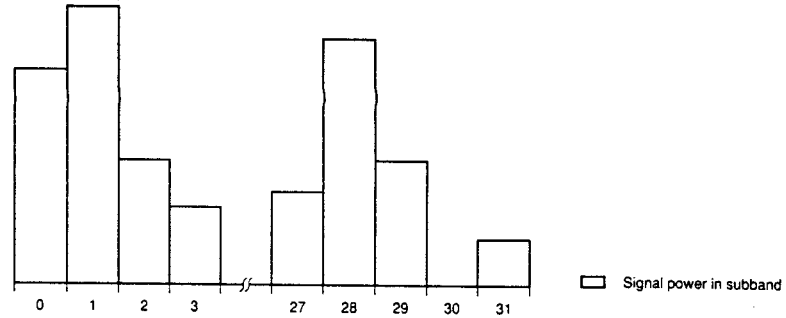
Extensive acoustic investigations have shown that in real sound spectra as well the masking threshold as the value of the subband samples itself change relatively slowly. Therefore, 12 successive (filtered) samples of a subband have been combined into one block.
The first step of the PASC-coding is to calculate the average signal power of these 32 subband blocks:

$$P_i = \frac{1}{12} \sum_{j=1}^{12} X_{i,j}^2$$

i..subband number (0..31)
j..subband sample index

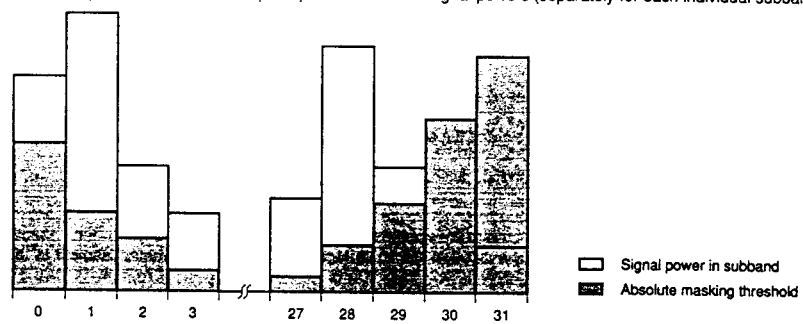
This formula represents precisely the square of the effective value for the discrete case.

For instance, the following power distribution could occur:



5.3. SUPERIMPOSING HEARING THRESHOLDS

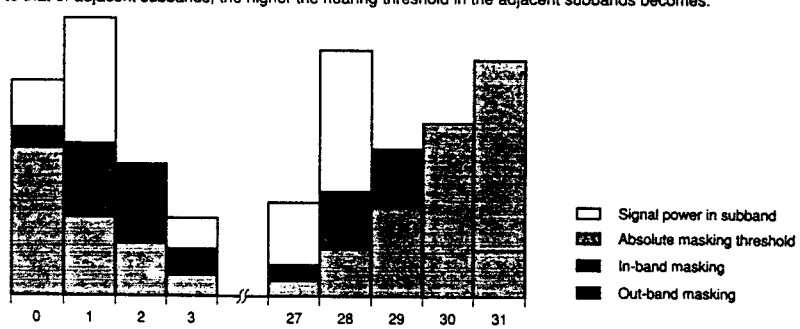
The hearing thresholds are now superimposed over these signal powers (separately for each individual subband):



It can be seen that in subbands 30 and 31 the signal power is below the hearing threshold. These signals are inaudible and therefore need not be coded.

5.4. IN-BAND AND OUT-BAND MASKING

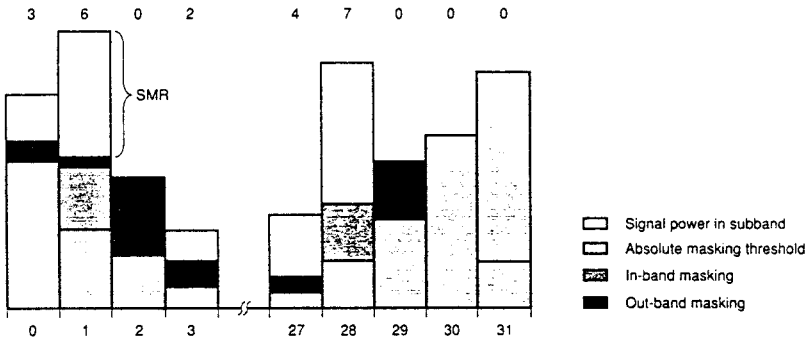
The next step is to calculate the masking power of the subbands. There are two different types of masking:
In-band masking: Masking of signals within the corresponding subband.
Out-band masking: Masking of signals in subbands at higher frequencies. The higher the signal power of a subband compared to that of adjacent subbands, the higher the hearing threshold in the adjacent subbands becomes.



In this example, after taking into account the hearing threshold and masking, only subbands 0, 1, 3, 27 and 28 are coded, and all the other data is discarded.

5.5. CALCULATION OF ALLOCATION INFORMATION

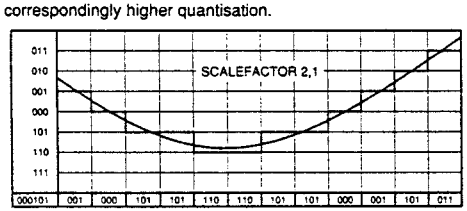
The greater the difference between the signal power and the hearing threshold, the more bits are allocated to the subband. The ratio between the signal power and the hearing threshold is called the signal to mask ratio (SMR). Up to 15 bits can be allocated. As it is pointless to use only one bit (the sign bit), the number of bits used is 0, 2, 3, 4 ... 15. The number of bits to be allocated per subband is calculated as n (SMR - 2dB) / 6dB.

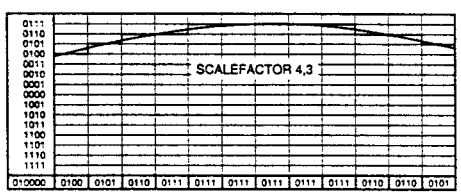


5.6. SCALING SUBBAND SAMPLES

After calculating the allocation information, the 12 samples of a subband are scaled, each sample beingrepresented in floating-point form, with a mantissa
(0..15 bits) and an exponent (6 bits). The exponent is also called the scale factor and only needs to be stored once per subband.
– The mantissa
is the numerical value of the sample. Its length corresponds to the calculated allocation of the respective subband, i.e. is represented by 2..15 bits.
– The scale factor
gives the height of the dynamic window which is used to acquire the sample of a subband. If the dynamic range is +6 to -118dB, and the number of bits is 6, 2dB steps are possible. The value of the scale factor depends on the greatest sample in the subband, the nearest 2dB step being chosen.

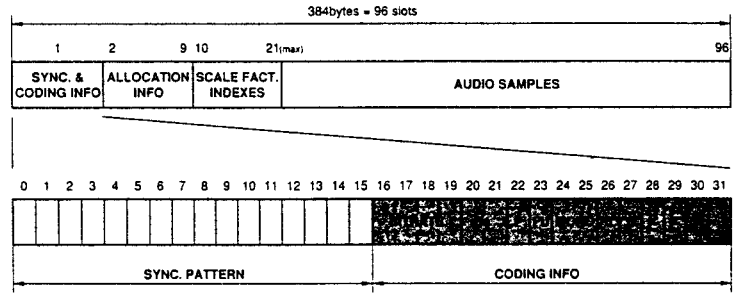
For rapidly changing waveforms, a small mantissa quantisation such as 3 bits (8 levels) is enough. Flatter signals need correspondingly higher quantisation.





5.7. PASC FRAME FORMAT

Each PASC frame includes the following information:
– allocation information for 32 subbands, each with 12 subband samples, 4 bits
– scale factor information for 32 subbands, each with 12 subband samples, 6 bits
– coded and scaled subband samples, 0..15 bits
– synchronisation pattern and additional information such as bit rate, sampling frequency, etc., 32 bits.


384bytes = 96 slots
1 2 9 10 21(max) 96
SYNC. & CODING INFO
ALLOCATION INFO
SCALE FACT. INDEXES
AUDIO SAMPLES
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
SYNC. PATTERN
CODING INFO

6. ERROR DETECTION AND CORRECTION

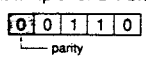
Digital signals are as liable to interference as analog signals. However, the effects of interference on a digital transmission path are much more critical than for analog signals. A wrongly transmitted MSB of a data word in 2s complement form results in a change of sign, so the information becomes quite different. Apart from such single bit errors, whole data words may be lost or falsified. Such cases are called "burst errors".
Depending on the cause of the interference, errors may be permanent (hard) or transient (soft). Permanent errors are caused by defects in the storage medium itself (e.g. damaged tape material) or the control circuits. Transient errors occur randomly and cannot be reproduced. They are mainly caused by alpha radiation and noise pulses.

6.1. PRINCIPLES OF ERROR DETECTION AND CORRECTION

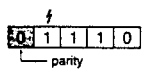
Before an error in a data signal can be corrected, it must be detected. However, bit errors in an n-position code cannot be recognised without special arrangements. To make this possible, one or more check bits must be stored, as well as the true data bits. The more check bits are used, the more errors can be detected and corrected.
The simplest method of error detection is the parity check. In this method, a correction bit P is added to the data word. The value of this parity bit is calculated by an EXOR (exclusive or) operation on the individual data bits. Parity may be even (parity bit = "0" if the number of "1" values in the original data word is even) or odd (parity bit = "0" if the number of "1" values in the original data word is odd).

Even parity requires following rules of calculation:
0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 0

Example for a 4-bit data word (even parity):

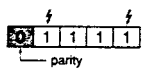


If a single bit error occurs, the following can be recognised:



The parity bit can be seen to be wrong, so the error is detected, but it cannot be localised.

If there are two wrong bits, the following bit pattern will be received:



This code word is recognised as correct, since the number of 1s is correct.

The simple parity check therefore has the following disadvantages:
- Errors are detected, but cannot be localised or corrected.
- The parity bit itself can be falsified, so that an error is reported, although the actual data was transmitted correctly.
- Multiple errors can only be detected if the number of errors is odd.

A significant improvement is achieved by using Hamming code, in which by adding k parity bits to m information bits a so-called error pointer is created which makes it possible to detect and localise a falsified bit.
The number of parity bits required is given by the formula $2^k \geq m+k+1$. (2^k different bit patterns can be formed from k check bits, so that with m data bits the total word length is m+k. An additional parity bit is required to show that the received data word is correct.) The following table shows the solutions which are important in practice:

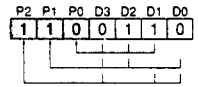
DATA	m	1-4	5-11	12-26	27-57	58-120	121-247
PARITY	k	3	4	5	6	7	8

It can be seen that the greater the number of data bits to be transmitted, the smaller the proportion of check bits in the total word length.

General points about Hamming code:
- The smallest number of bits by which two legal code words differ is called "Hamming distance", and is calculated as HD = k+1.
- The maximum number of detectable errors depends on HD, and is defined by tmax = HD-1.
- The maximum number of correctable errors is defined by emax = (HD-1) / 2.

According to the table above, for 4 data bits 3 parity bits are necessary.

Example for a simple error coding of 4 data bits:

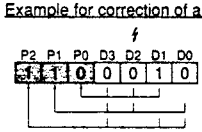


The parity bits P0..P2 are calculated as follows:
P0 = D1 + D2 + D3 = 1 + 1 + 0 = 0
P1 = D0 + D2 + D3 = 0 + 1 + 0 = 1
P2 = D0 + D1 + D3 = 0 + 1 + 0 = 1

With this code, it is possible to localise errors. A defective bit can be localised as follows:
f1 = D0 + D2 + P0 + P2 = 0 + 1 + 0 + 1 = 0
f2 = D1 + D2 + P1 + P2 = 1 + 1 + 1 + 1 = 0
f3 = D3 + P0 + P1 + P2 = 0 + 0 + 1 + 1 = 0

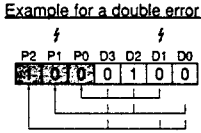
f3 f2 f1 indicates an error pointer (binary coded), which shows the digit to be corrected.
"000" means, that no error has been detected, "001" indicates an error in the 1st data bit (= D0), "010" an error in the 2nd data bit (= D1), and so on. It is also possible to detect a error in the parity bit.

Example for correction of a single error in data bit D2:



The error pointer is calculated as follows:
f1 = D0 + D2 + P0 + P2 = 0 + 0 + 0 + 1 = 1
f2 = D1 + D2 + P1 + P2 = 1 + 0 + 1 + 1 = 1
f3 = D3 + P0 + P1 + P2 = 0 + 0 + 1 + 1 = 0
An error has been localised in the 3rd data bit (= D2).
In a binary code a localised error can be corrected simply by negating it.
After correction the bitstream will be "110 0110" – the original code word has been reconstructed.

Example for a double error in P1, D1:



The error pointer is calculated as follows:
f1 = D0 + D2 + P0 + P2 = 0 + 1 + 0 + 1 = 0
f2 = D1 + D2 + P1 + P2 = 0 + 1 + 0 + 1 = 0
f3 = D3 + P0 + P1 + P2 = 0 + 0 + 0 + 1 = 1
The error pointer shows an error in the 4th data bit (= D3), the douple error could not be detected.
The corrected bitstream will be "100 1100" – a totally false code word!

For a Hamming distance of 3:
- Single and double errors are always detected, but not all triple errors.
- Single errors can be localised (and therefore corrected). Double errors are always falsely corrected, since the assigned code word is always wrong!

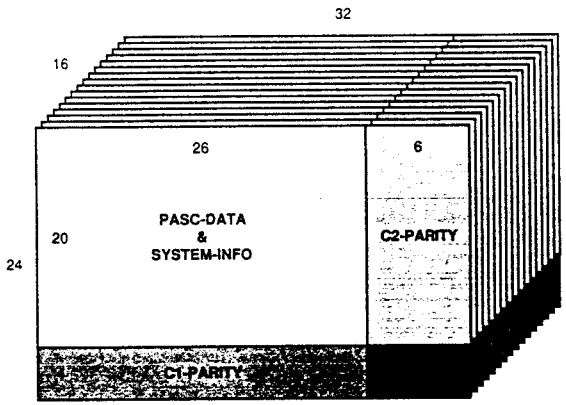
Since false error correction is possible, if it occurs the remaining error rate is greater than with error detection only, so error correction must be used with caution.

6.2. ERROR DETECTION AND CORRECTION IN THE DCC SYSTEM

The DCC system has a much more powerful method of error correction. For the main and AUX data, two different error coding algorithms are used.

6.2.1. ERROR CORRECTION FOR MAIN DATA

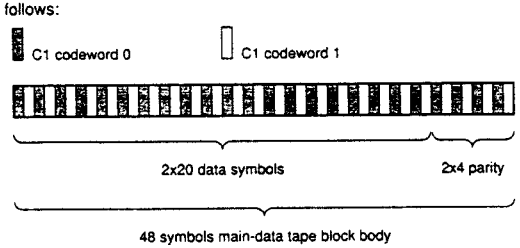
The 8 main data tracks are protected by a two-stage coding, consisting of the "Cross interleaved Read Solomon codes" (CIRC) C1 and C2.
C1 is 24 bytes long, of which 20 are information bytes and 4 are parity bytes. The Hamming distance is 5, so that with C1 alone 4 errors can be detected.
C2 is 32 bytes long, of which 26 are information bytes and 6 are parity bytes. The Hamming distance is 7, so that with C1 alone 6 errors can be detected.
The C1 and C2 parity bytes are formed from the rows and columns of a matrix. This produces an additional product code C1/C2, which further increases the efficiency of the individual codes.



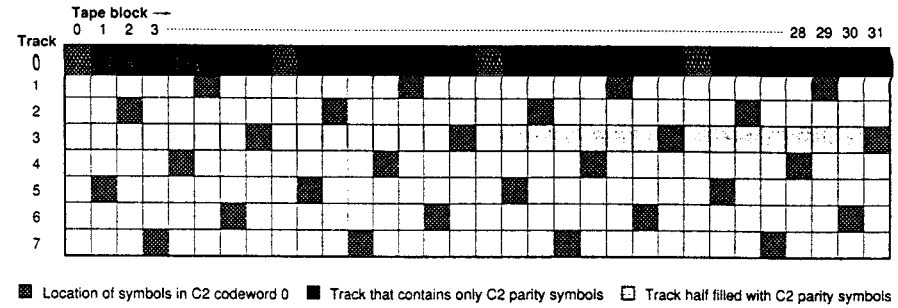
First, 16 matrices are formed, each from 20 x 26 main data (PASC and Sysinfo). From the 20 rows, 4 C1 parity bytes are calculated, and from the 26 columns, 6 C2 parity bytes are calculated. Subsequently, 24 C1/C2 product bytes are formed. For each matrix, the result is:

```
  520  bytes main data
  104  bytes C1
  120  bytes C2
   24  bytes C1/C2
  ---
  768  bytes per Matrix
x  16
  ---
12288  bytes
```

These 12288 bytes form a tape frame block, which is written on tape in interleaved form. The C1 code words are distributed as follows:



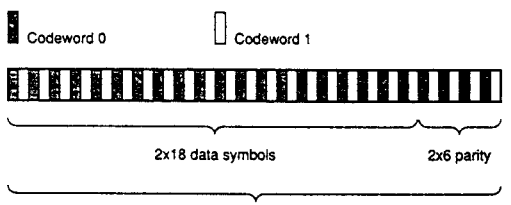
The C2 code words are arranged as follows on the tape:



Because of the honeycomb-like interleaving of the C2 codes, an optimum physical distribution of the symbols is achieved. Data losses up to a diameter of 1,45mm, and even the loss of a complete data track, can therefore be corrected without affecting the sound.

6.2.2. ERROR CORRECTION FOR AUX DATA

AUX data is recorded on one track only. This limits the coding possibilities. For this reason, the data rate of the AUX data was reduced to 1/8 of the main data rate (12kbit/sec). The CIRC which is used consists of 7 C1 code words, from which up to 6 errors can be detected. The data is interleaved as follows:



6.3. CHANNEL CODING

The data produced as described above is a sequence of "0"s and "1"s, which cannot be simply stored on tape without special processing, but must first be adapted to the properties of the transmission channel. The channel coding must meet the following requirements:

- It should be free of DC voltage and have no low frequency signal components (so on average the number of "0"s transmitted must be the same as the number of "1"s).
- Since no additional clock signal is transmitted, the clock must be recovered from the edges of the data signal. For DCC, the maximum number of equal data bits in succession is 5.
- The code used must be adapted to the error correction code used.

For DCC, eight to ten modulation (ETM) is therefore necessary. In this coding method, a 10-bit word is assigned to each 8-bit data byte. Of the 2^{10} possible combinations, only those which meet the requirements of channel coding are used (so code words with 6 or more successive equal bits are immediately excluded). But even the remaining code words represent different DC levels, which would appear in the data channel as low-frequency oscillations. To minimise this effect, the data byte to be coded must be adapted to the previously transmitted code word. For this reason, for each 8-bit word there are two possible corresponding 10-bit words, one with positive DC level, one with negative (apart from a few exceptions where the "01"-sequence is completely DC neutral). Which 10-bit word is actually selected is decided by the so-called DSV (digital sum value) bit. This bit is "1" if more "1"s have been transmitted previously, and "0" if more "0"s have been transmitted, and is updated after each transmitted word.
In the IC, the conversion is done according to a table. The following extract shows possible assignments of the10-bit symbols, according to the input byte and the DSV value of the last data word to be transmitted (old DSV).

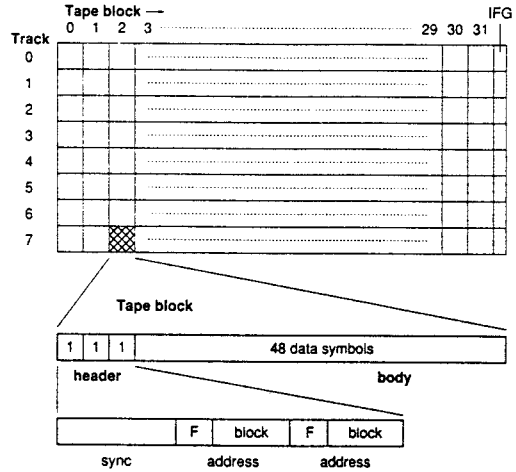
			EIGHT TO TEN MODULATION TABLE							
INPUT BYTE			S0 TABLE (old DSV=0)				S1 TABLE (old DSV=1)			
DEC	HEX	BINARY	DEC	HEX	BINARY	DSV	DEC	HEX	BINARY	DSV
0	00	00000000	171	0AB	0010101011	0	171	0AB	0010101011	1
1	01	00000001	173	0AD	0010101101	0	173	0AD	0010101101	1
2	02	00000010	174	0AE	0010101110	0	174	0AE	0010101110	1
3	03	00000011	179	0B3	0010110011	0	179	0B3	0010110011	1
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
89	59	01011001	175	0AF	0010101111	1	43	02B	0000101011	0
90	5A	01011010	303	12F	0100101111	1	45	02D	0000101101	0
91	5B	01011011	559	22F	1000101111	1	46	02E	0000101110	0
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
98	62	01100010	183	0B7	0010110111	1	75	04B	0001001011	0
99	63	01100011	311	137	0100110111	1	77	04D	0001001101	0
100	64	01100100	567	237	1000110111	1	78	04E	0001001110	0
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
254	FE	11111110	632	278	1001111000	0	121	079	0001111001	1
255	FF	11111111	868	364	1101100100	0	155	09B	0010011011	1
SYNC WORD			318	13E	0100111110	1	62	03E	0000111110	1

7. RECORDING DATA ON TAPE

Two kinds of data are transmitted in DCC systems:

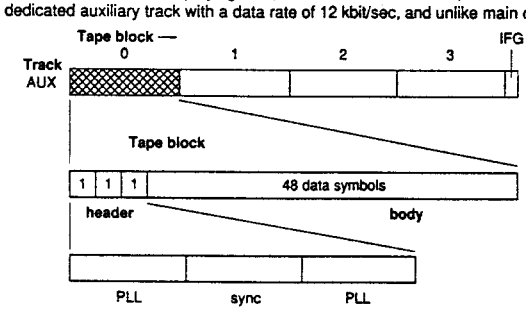
– Main data
includes the true PASC data, plus so-called system information (sysinfo). Sysinfo is continuously added to the PASC data, and includes the status of the Copyright Management System (SCMS), the recording format, and text information on pre-recorded tapes. Main data is recorded on 8 data tracks, each with a data rate of 96 kbit/sec.

Each of the 8 main data tracks contains 32 tape blocks per frame.



A tape block consists of 51 tape symbols, each of 10 bits (ET modulated).
The first 3 symbols (30 bits) of a tape block are the so-called "block header", which in turn consists of a sync pattern (which identifies the start of a block), a 3-bit frame address, and a 5-bit block address. The remaining 48 symbols contain the actual PASC and sysinfo data and are called the "tape body". The frame and block addresses are necessary so that the received data can be written to the correct RAM locations for decoding and error correction.

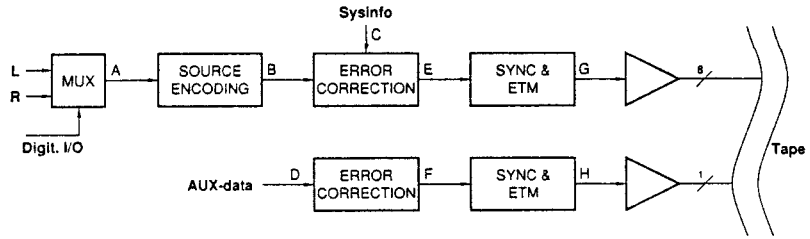
– AUX data
includes information like playing time, track and index numbers, and markers for search, reverse, etc. AUX data is recorded on a dedicated auxiliary track with a data rate of 12 kbit/sec, and unlike main data it can be modified subsequently.



7.1. INTER FRAME GAP

Two adjacent tape frames are separated from each other by a so-called inter frame gap (IFG). The purpose of the IFG is to compensate for differences between the external EBU clock frequency and the internal master clock frequency, which occur during digital recording. If the two frequencies are the same, the IFG is 64 bits long. If the external clock frequency is higher, the IFG is correspondingly shorter, and vice versa. The maximum length of the IFG is 96 bits, and the minimum is 31 bits. Clock frequency differences of 0,2% are therefore possible. The clock precision of the EBU signal is specified as 0,05%, so that fluctuations can easily be absorbed by the IFG.
Because of the lower data rate, the IFG of the AUX channel is only 8 bits long.

7.2. DATA RATES OF THE DCC SYSTEM



A : 16bits per sample and channel on the input side

16 x 2 x fs	fs = 32kHz	1024 kbit/s
	fs = 44,1kHz	1411,2 kbit/s
	fs = 48kHz	1536 kbit/s

B : Source coding PASC (subband I²S)

	fs = 32: 44,1; 48kHz	384 kbit/s

C : Sysinfo — 6 kbit/s

D : AUX-Data — 6,75 kbit/s

E : C1 + C2 Reed Solomon (main data & sysinfo)
Rate 20/24; 26/32
(24/20) x (32/26) x (384 + 6 kbit/s) = 576 kbit/s

F : Reed Solomon (AUX-data)
Rate 18/24
(24/18) x 6,75 kbit/s = 9 kbit/s

G : Main data
ETM (8/10), Synchronization (48/51), IFG 0,4%
(10/8) x (51/48) x 1.004 x 576 kbit/s = 768 kbit/s
(8 x 96 kbit/s)

H : AUX data
ETM (8/10), Synchronization (48/51), IFG 0,4%
(10/8) x (51/48) x 1.004 x 9 kbit/s = 12 kbit/s

It follows that:
duration of a tape frame: about 170 msec
length of a tape frame: about 8,1mm
bit length on tape: about 500nm for main data tracks, 4m for AUX track

8. SOFTWARE FEATURES

As already mentioned, not only digital audio data is recorded on a DCC, but also a range of additional information, some intended for the microprocessor (sampling frequency, copyright, emphasis, etc.), and some to increase user-friendliness. This additional information is partly included in the main data (where it is called sysinfo), and partly in the AUX track (where it is called AUX data).

There are 4 principal types of DCC recording:
- **pre-recorded 2-sector tape**
  is a pre-recorded tape, which is commercially available and has the features of a CD and extras such as album and song titles, song texts, etc. It is called "2-sector" because two stereo channels are recorded on each side (sector).
- **pre-recorded 4-sector tape**
  is similar to pre-recorded 2-sector tape, but has 2 mono channels recorded on each side. Used, e.g., for language courses.
- **user tape**
  can be used for the consumer's own recordings. Each recording can begin at any arbitrary point. User Tape has few features.
- **super user tape**
  is an enhancement of user tape, and provides additional features such as track numbers, time information and table of contents (TOC).

8.1. SYSTEM INFORMATION

Sysinfo is a part of main data and is recorded at the same time as the audio signal. Unlike AUX data, sysinfo cannot be changed without simultaneously changing the music data.
A tape frame (12288 bytes) contains 128 bytes of sysinfo, which contain the following information:
- copyright protection bits
- text information (on pre-recorded tapes only)
- type of recording (pre-recorded 2-sector or 4-sector tape, user tape, super user tape)
- other data still to be defined.

8.1.1. TEXT INFORMATION

Text can be displayed in 3 different formats:
- 1 line of 12 characters
- 2 lines of 40 characters
- 21 lines of 40 characters.

The following information can be shown on the 1-line display:
- album title
- track title
- name of performer of current track.

On the 2-line or 21-line display:
- album title
- track title
- list of song titles
- name of performer of current track and credits
- optionally, various additional information
- song texts synchronised with music
- optionally, text can be shown in any of 7 languages.

21-line displays are unlikely to be used in DCC devices, but the text information can be shown on a computer monitor or TV, via an appropriate interface.

8.2. AUX DATA

AUX data is recorded on a dedicated AUX track, and can be modified without changing the music data. The AUX track can be overwritten during either recording or playback. The AUX channel contains the following data:
- track numbers, time information and table of contents
  Tracks are numbered as for CDs (track and index numbers).
  Time information includes absolute playing time, track playing time, remaining total playing time and remaining track playing time, and is given in hours, minutes and seconds.
- data which results in the DCC recorder carrying out specified actions. This information is called "marker", and is described in more detail in 8.2.2.
- additional information.

8.2.1. TRACK NUMBERS AND TIME INFORMATION

Whether this information is on the tape, and if so to what extent, depends on the type of recording:

– PRE-RECORDED 2-SECTOR TAPE

Track numbers give the number of the current musical item, or of the previous pause. Track numbering begins on sector A at 01, and ends with the number of the last item on sector B.
Index numbers further divide a track into smaller sections. Index numbering begins with 00 during the pause, is 01 at the start of the title, and increases continuously. At the next pause between two tracks, the index number is reset to 00.
Chapter numbers group several tracks into a larger section.
Absolute playing time begins at the start of the tape (sector A) at 00.00.00, and increases continuously to the end of sector B.
Remaining playing time is total playing time minus absolute playing time.
Track playing time begins at the start of the musical item at 00.00, and increases continuously to the end of the track. The length of the pause between two tracks is displayed, and decreases until the start of the next track.
Remaining track playing time is the total playing time of the current track minus track playing time.

– PRE-RECORDED 4-SECTOR TAPE

Track, index and chapter numbers are always 00 on playback, because unique assignment of the musical items is not possible.
Absolute and remaining playing time as for pre-recorded 2-sector tape.
Track playing time and remaining track playing time are not recorded, for the reasons given above.

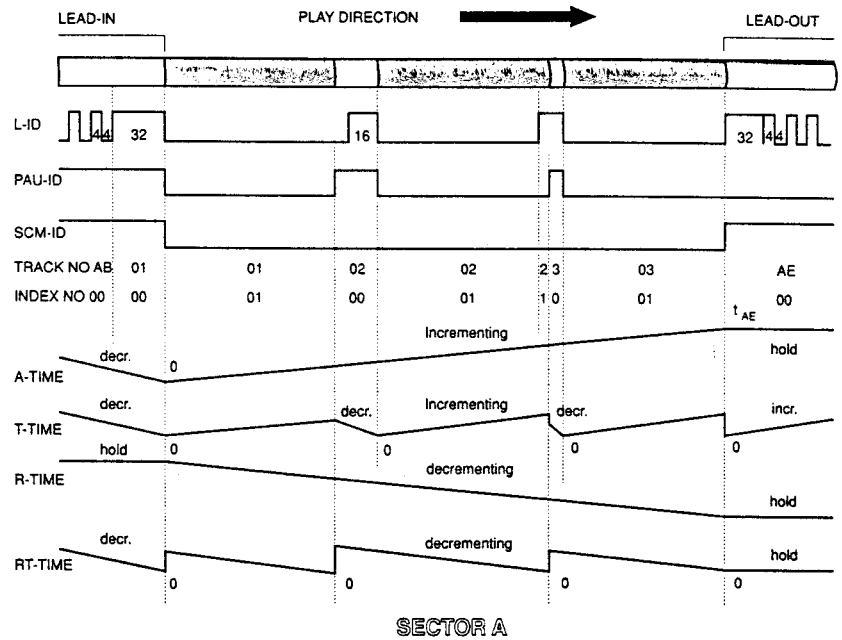
– USER TAPE

Track numbers are always 00 on playback.
Index numbers are not recorded.
Chapter numbers can be assigned only at the start of a track, together with start markers.
Playing times are not recorded.

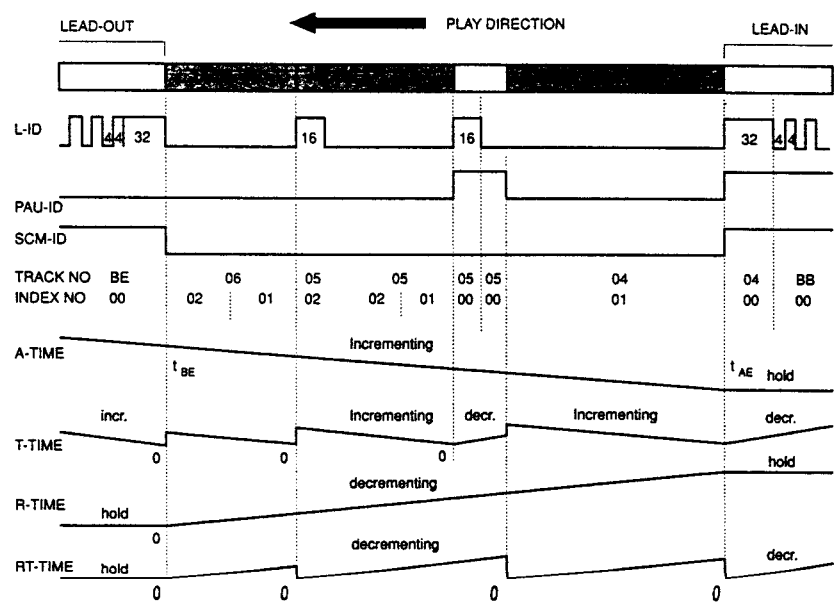
– SUPER USER TAPE

Track numbers are recorded only at the start of a track, together with start markers, since if a new recording is made, e.g. in the middle of an existing track, all following track numbers must be raised by 1 (renumbered).
Index numbers are not recorded.
Chapter numbers can be assigned only at the start of a track, together with start markers.
Absolute and remaining playing times as for pre-recorded tape.
Track playing time starts at 00.00 and increases continuously. Pauses are displayed only for CD copies.
Remaining track playing time is not displayed.

OVERVIEW OF DATA ON PRERECORDED 2-SECTOR TAPE

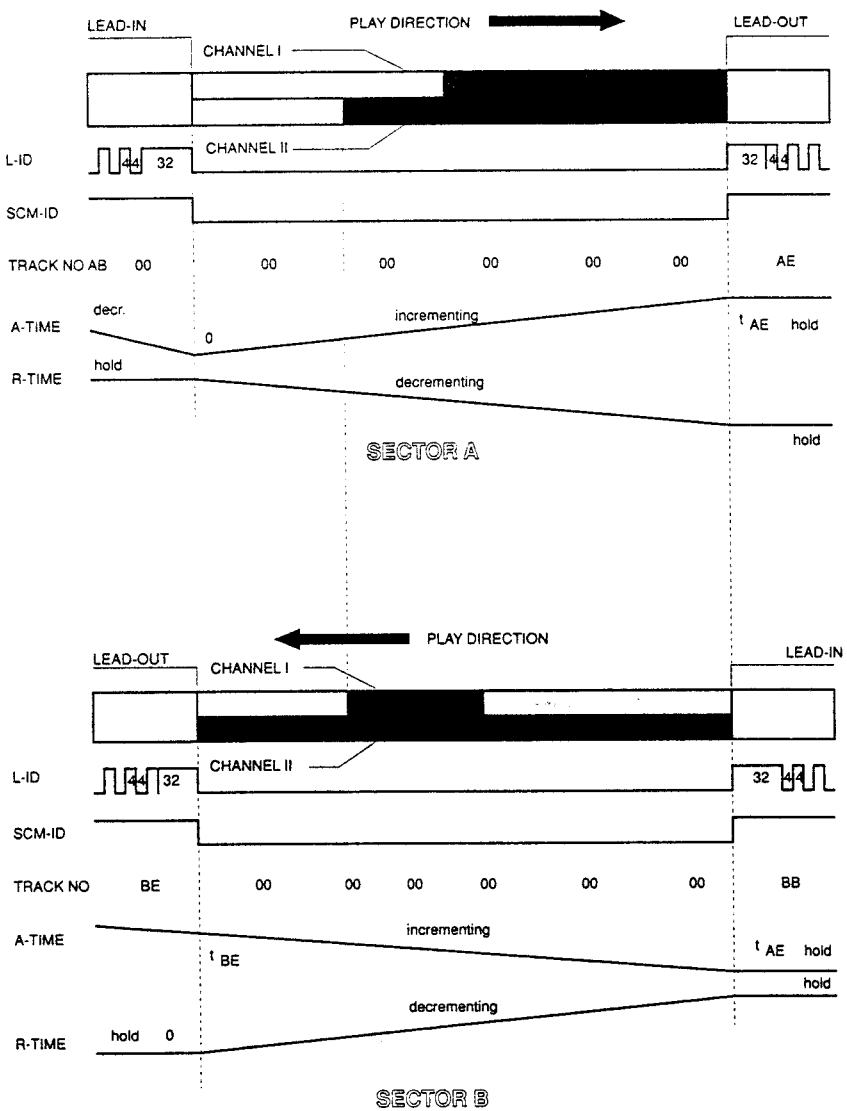


SECTOR A

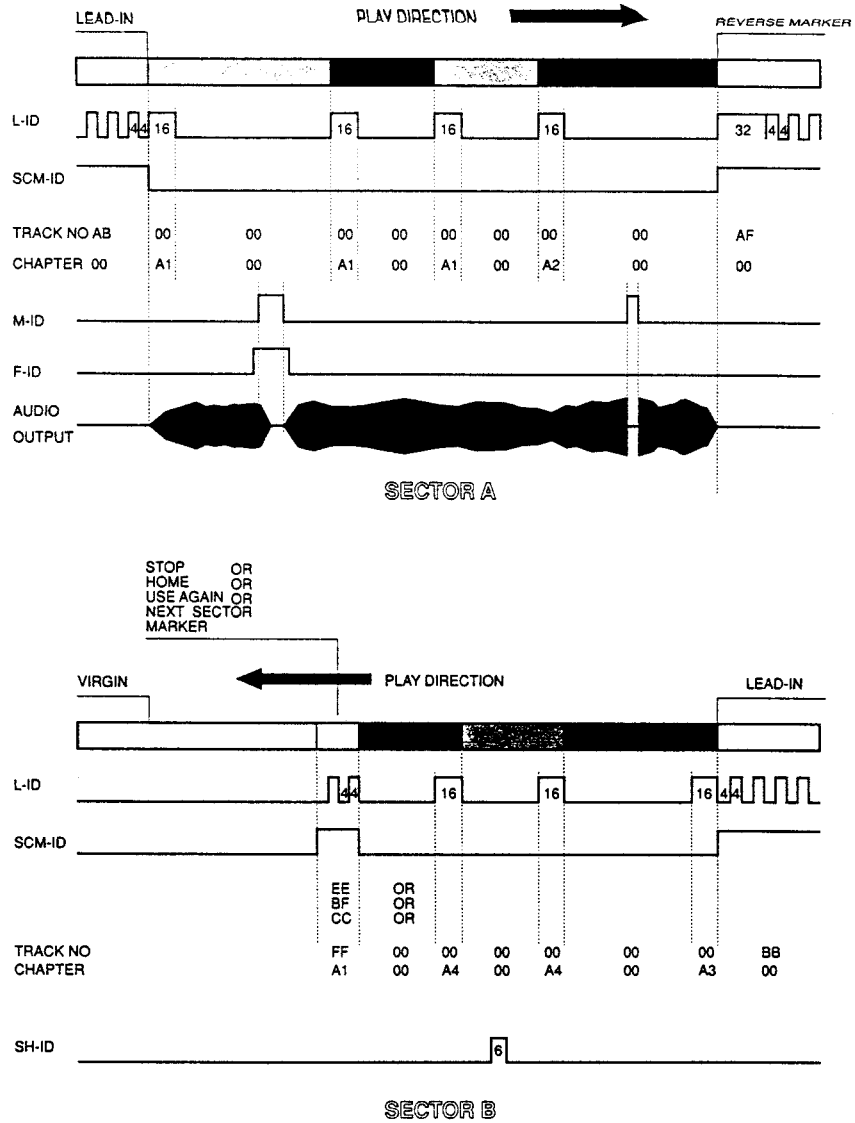


SECTOR B

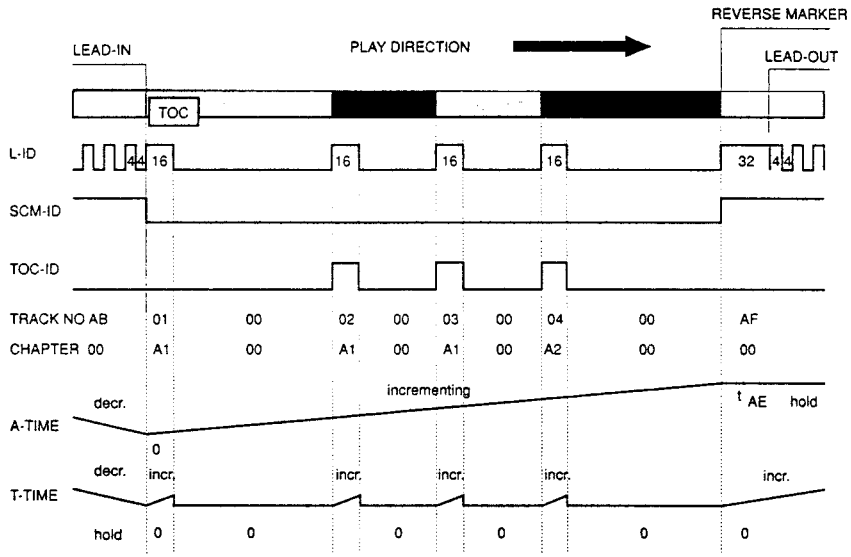
OVERVIEW OF DATA ON PRERECORDED 4-SECTOR TAPE



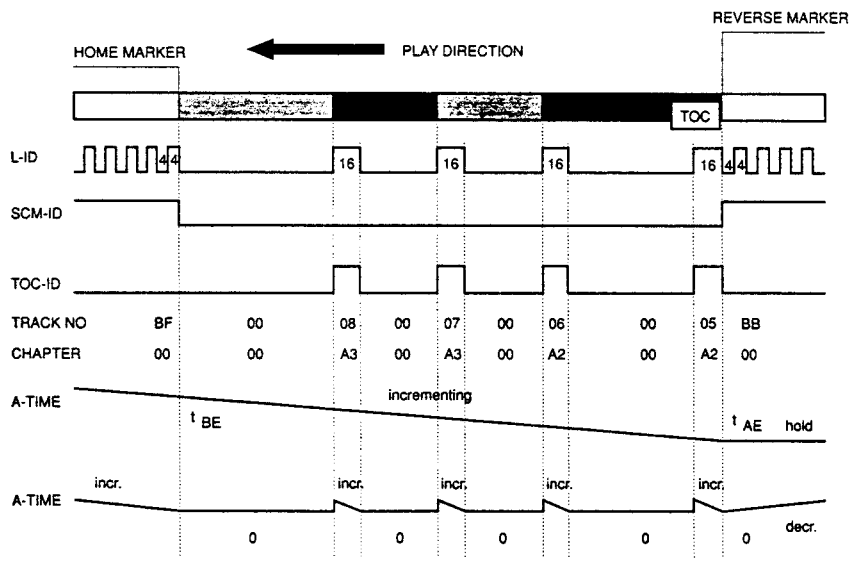
OVERVIEW OF DATA ON USER TAPE



OVERVIEW OF DATA ON SUPER USER TAPE



SECTOR A



8.2.2. MARKERS

Markers are information in the AUX channel which results in the DCC recorder carrying out specified actions, or which it needs to function correctly.
There are 3 distinct types of marker, called start, sector and feature markers. Start and sector markers can be detected in both playback and search mode.

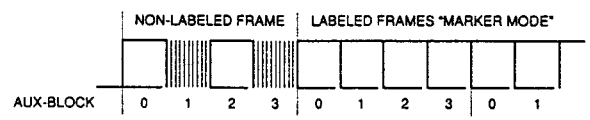
The following markers can appear, depending on the recording type:

	Prerecorded 2-Sector Tape	Prerecorded 4-Sector Tape	Customer rec. Super user tape	Customer rec. User tape
Start-Marker	x	n.a.	x	x

Sector-Markers	Prerecorded 2-Sector Tape	Prerecorded 4-Sector Tape	Customer rec. Super user tape	Customer rec. User tape
Lead-in	x	x	x	x
Lead-out	x	x	x	x
Reverse-Marker	n.a.	n.a.	x	x
Next-Marker	n.a.	n.a.	x	x
Home-Marker	n.a.	n.a.	x	x
Stop-Marker	n.a.	n.a.	x	x
Use again-Marker	n.a.	n.a.	x	x

Feature-Markers	Prerecorded 2-Sector Tape	Prerecorded 4-Sector Tape	Customer rec. Super user tape	Customer rec. User tape
Skip-Marker	n.a.	n.a.	x	x
Mute-Marker	n.a.	n.a.	x	x
Fade-Marker	n.a.	n.a.	x	x

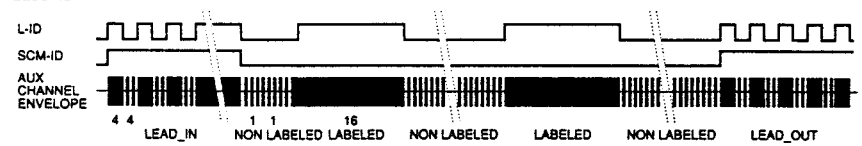
Each marker is identified by a special pattern in the AUX channel. The AUX information is stored on the tape in so-called AUX frames, which in turn consist of 4 AUX blocks.



If all 4 blocks (header and body) are recorded, it is called a "labelled frame", if only the even-numbered AUX bodies are recorded, it is a "non-labelled frame".

In search mode, the tape speed increases to 3..50 times the normal speed of 4,76 cm/sec. Therefore, in search mode no data can be read, but the different envelopes of labelled and non-labelled frames can be recognised, and evaluated by the microprocessor. However, for this purpose the current tape speed must be known. It can be determined by two light barriers under the winding disks in the drive.

Label-ID

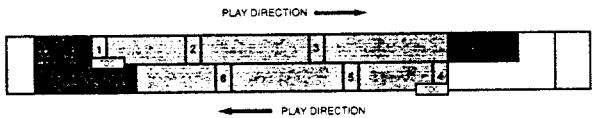


8.2.2.1. START MARKER

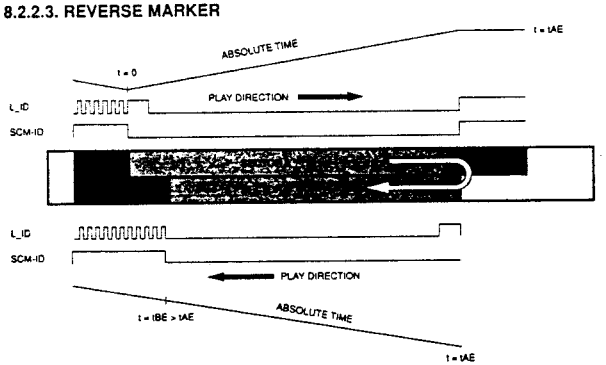
Start markers are placed in the music program area and mark the start of a new music track.
Two different start marker can appear, depending on the recording type:
- Prerecorded tapes: The length of a start marker is 16 labeled frames. Start markers are recorded 16 frames before the start of music.
- Customer recorded tapes: The length of a start marker is either 16 or 32 labelled frames. Start marker with a length of 32 labeled frames are the result of a renumber action, and may only occur on sector B. The length of 32 frames makes it possible to use the marker also as indication for a continued recording from sector A to B (especially useful in backwards search on sector B).

8.2.2.2. SECTOR MARKER

The main purpose of sector markers is to mark the start and end of a music program area. The following sector markers are defined:
- lead-ins mark the start of a sector, A or B
- lead-outs mark the end of a sector, A or B.

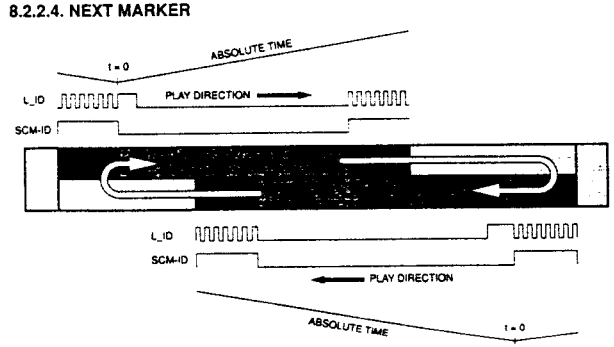


8.2.2.3. REVERSE MARKER



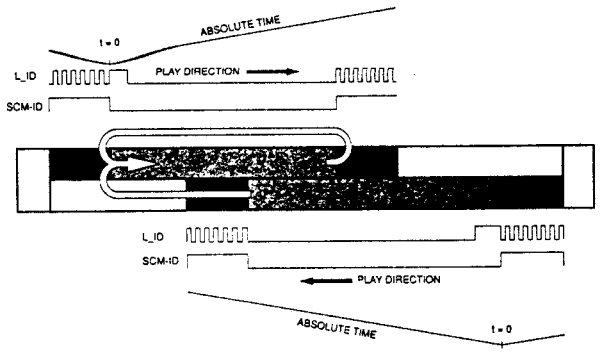
The reverse marker marks a point on sector A, from which the DCC recorder is to change to sector B. This marker can only exist on sector A.

8.2.2.4. NEXT MARKER



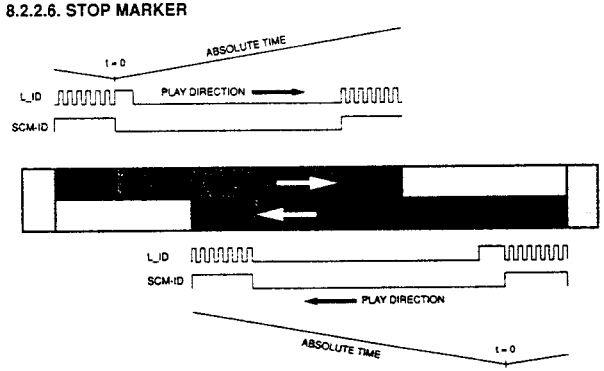
The next marker causes the DCC recorder to wind to the start of the next sector, and either to stop there or to begin playback, depending on the selected repeat mode.

8.2.2.5. HOME MARKER



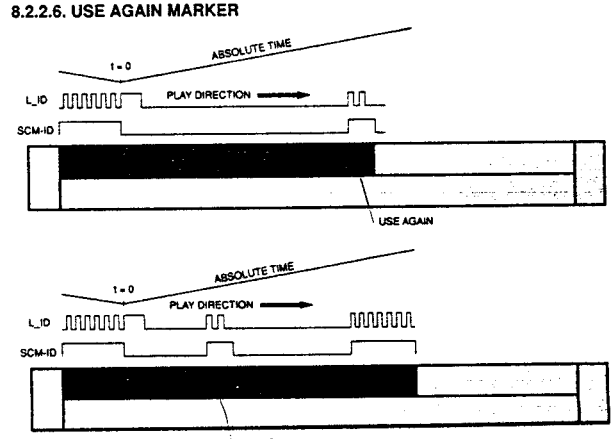
The home marker causes the DCC recorder to wind to the start of sector A.

8.2.2.6. STOP MARKER



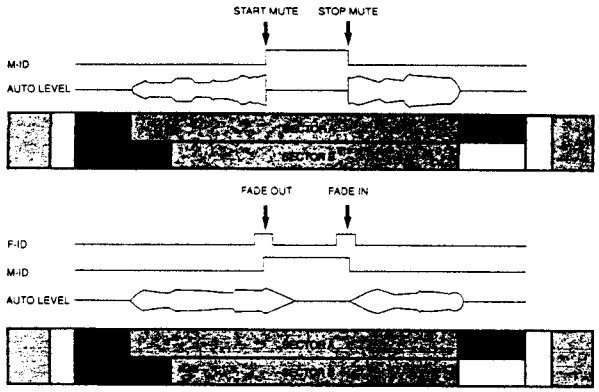
The stop marker causes the DCC recorder to stop at the marked place on the tape.

8.2.2.6. USE AGAIN MARKER



The use again marker is written on super user tapes, at the end of the last recording. If the Append key is pressed, the recorder searches for this marker, to add a new recording. At the end of the recording, a new use again marker is written. It is thus possible to write time and track information to the tape.

8.2.2.8. FEATURE MARKER



Feature markers cause the DCC recorder to mute, to fade the start or end of a track, or to wind to the next track. Feature markers are only effective during playback.

8.2.3. ADDITIONAL INFORMATION

The following additional information is contained in the AUX channel:
- International Standard Recording Code (ISRC) (12 characters)
- catalogue number code (UPC/EAN) (13 characters)
- recording date (year-month-day-hours-minutes-seconds)
- remaining track playing time
- customer character code

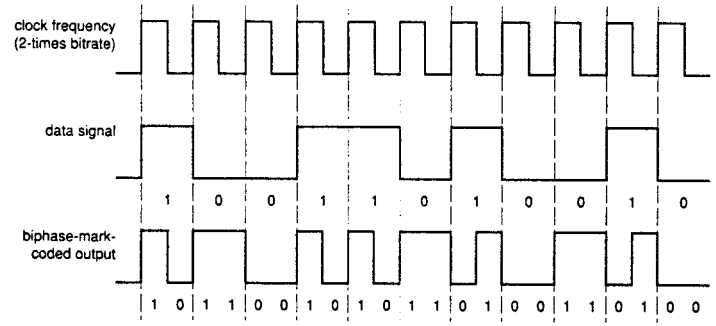
Any text can be stored here (e.g. the title of a personal recording). The customer character code is recorded with a start marker.

9. DIGITAL OUT

The digital interface enables serial, digital stereo data signals to be transferred at a quantisation of up to 24 bits. The signal at the cinch socket of a digital output is free of DC voltage; it consists of superimposed sinusoidal AC voltages (eye diagram) with an amplitude of 500mVss. The data rate depends on the sampling frequency, and is 2,8224 Mbit/sec for CD, 3,072 Mbit/sec for DAT, and 2,048 Mbit/sec for digital broadcast. All impedances (output, cable, input) are fixed at 75Ω.

9.1. BIPHASE MARK CODE

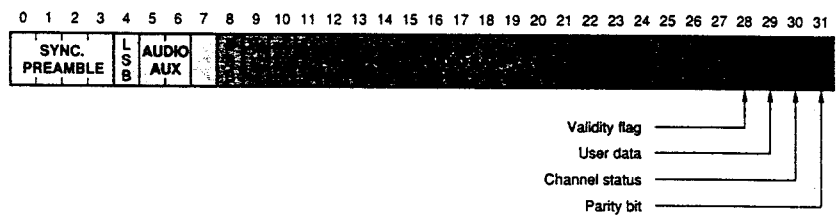
The digital audio data is coded in biphase mark code, which is a form of two phase modulation. In this form of transmission, a logical 1 is represented by two changes of polarity of the signal (zero crossings), and a logical 0 is represented by only one change of polarity. The clock rate is therefore twice the bit rate.

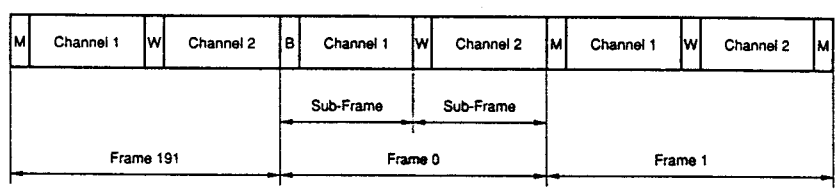


Each data bit to be transmitted is represented by two successive states (effectively by two bits), which together form a "cell". A cell corresponds to the timeslot for a data bit. The logical state at the start of a timeslot is always the opposite of the state at the end of the previous timeslot. The logical state at the end of the data bit is unchanged if the bit to be transmitted is "0", and the opposite if it is a "1". Therefore
- the polarity of the signal changes after each bit
- the polarity changes twice for a "1".

32 bits (= 1 subframe) are transmitted for each audio sample. Two of these subframes, one for channel I (left) and one for channel II (right), form a frame. 192 successive frames form a block.

9.2. FRAME FORMAT


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
SYNC. PREAMBLE
LSB
AUDIO AUX
Validity flag
User data
Channel status
Parity bit



TIMESLOTS 0..3 ("SYNC. PREAMBLE")

The first 4 bits of a subframe form a so-called "preamble", which is for synchronisation. This is necessary because no additional clock signal is transmitted, so the clock must be recovered from the data signal. The preamble can take three different bit patterns, which also identify the following data word or block. The three bit patterns have the following meanings:
- Preamble B marks a data word of channel I (left for stereo), at the start of a block.
- Preamble M marks a data word of channel I, not at the start of a block.
- Preamble W marks a data word of channel II (right for stereo). In multiple channel systems, preamble W can also be used for other channels (except I).

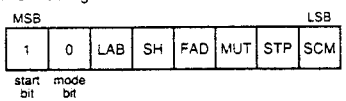
TIMESLOTS 4..7 ("AUDIO AUX")
Bits 4..7 contain the so-called auxiliary sample bits. These bits are used if samples are transmitted with 24-bit quantisation. If the resolution is less. these bits are set to 0. The MSB of a sample is always in timeslot 27.

TIMESLOTS 8..27 ("AUDIO SAMPLE")
Bits 8..27 contain the audio data. The MSB of a sample is always in timeslot 27, even if a lower quantisation is used.

TIMESLOT 28 ("VALIDITY FLAG")
This bit is called the "validity bit" or "error flag", and indicates to the receiver that the transmitted data word should not be used. For example, it is set to 1 if the output data is wrong.

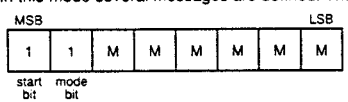
TIMESLOT 29 ("USER DATA")
In DCC, this bit is used for transmission of various user data. Two modes are available: "marker mode" is mandatory, "extended mode" is optional. A message consists of one or more information units. An information unit contains 8 bits. The first bit is called "start bit" and always "1". The remaining 7 bits contain the user-information.
Information units that belong to the same message are separated by less than or equal to 8 logical "0"-bits. Different messages are separated by more than 8 logical "0"-bits.

Marker mode
The message in marker mode consists of one information unit. The 8 bits have the following meaning:



The first bit ("start bit") is always "1".
The second bit is called "mode bit" and "0" to identify the marker mode.
LAB, SH, FAD, MUT and SCM are direct copies of the bits 2 and 4..7 in the marker info byte (AD1) of the AUX-code.
STP = "1" indicates that no audio signal is available (due to search actions or in stop mode). Otherwise this bit is "0".
The marker message must be sent once for every DCC tape frame.

– Extended-Mode
In this mode several messages are defined. The first information unit of a message ("header") is as follows:



The first bit ("start bit") is always "1".
The second bit ("mode bit") is "1" to identify the extended mode.
The 6 M-bits indicate the so-called "message-nummer" and have the following meaning:
000000 Current status of the DCC-set
000001 ITTS-packet start or complete packet
000010 ITTS-packet continuation
000011 ITTS-packet continuation and end

Status data contain information on the current mode of operation of the DCC-set, played sector, CC or DCC playback, and so on. The complete message (inclusive header) requires 5 information units.

ITTS-packets as recorded in the sysinfo bytes can optionally be transferred on the digital output. If sent, the message "000000" (current status) must also be implemented. All ITTS-packets have to be transmitted in the same sequence as recorded in the sysinfo. In total the extended message will consist of a maximum of 66 information units.

TIMESLOT 30 ("CHANNEL STATUS")
This bit is one of the 384 channel status data bits per block. Since the channel status data bits in both subframes are identical, there are really only 192 status bits per block. These 192 bits have the following meaning:

– Bits 0..7
form a control word. Bits 0 and 1 are always 0. Bit 2 is the "C bit" or "copy blocking bit". Bits 3..5 indicate whether the audio signal was recorded with ("100") or without ("000") emphasis.

– Bits 8..15
form the so-called "category code". The following codes are defined:
0000000 general
01100xx actual A/D converters
100xxxx laser optical products
110xxxx magnetic products
001xxxx digital broadcast
101xxxx musical instruments
01101xx future A/D converters
0001xxx solid state recorders
0000001 experimental products
010xxxx D/D converters
0111xxx digital broadcast
Bit 15 is called the L-bit, and is 0 if the audio signal is from an original source.
The category code for DCC devices is "1100001L".

– Bits 16..19
give the "source number":
0000 not specified
1000 source number 1
0100 source number 2
1100 source number 3
.
.
.
1111 source number 15

– Bits 20..23
give the "audio channel number":
0000 not specified
1000 channel A (left for stereo)
0100 channel B (right for stereo)
1100 channel C
.
.
.
1111 channel O

– Bits 24..27
give the sampling frequency:
0000 44,1kHz
0100 48kHz
1100 32kHz

– Bits 28..29
give the clock precision:
00 level II : ±50ppm
01 level III: ±1000ppm
10 level I : variable pitch

– Bits 30..191
are reserved for future use (usually "0").

TIMESLOT 31 ("PARITY BIT")
This bit is the even parity bit. Parity applies to timeslots 4..31 only, not the preamble.

10. Serial Copy Management System (SCMS) in DCC devices

According to the DCC standard, every DCC device must be fitted with SCMS. This applies even to devices without a digital output! SCMS allows any number of digital copies of original sound carriers, but prevents further digital copies of these "master tapes". Copies of master tapes can then only be made via a D/A → A/D conversion, but this results in loss of quality.

According to audio interface standard IEC958, every digital source is identified by with an 8-bit "category code" (see 9. "Digital out"). Bit 15 (timeslot 30) is called the L-bit, and indicates whether the digital signal is from an original source (L = "1") or a personal recording or "home copy" (L = "0").

Also, a so-called "control code", which gives the transmission mode and the copy protection status of the digital signal, is transmitted. The transmission mode is given by bits 0 and 1 of the channel status word. The copy status is given by bit 2 (the C-bit), which is 0 for protected material and 1 for unprotected material.

On the tape, 4 bits define the copy status:
- CP1 (copy bit 1) gives the copy protection status, and is the inverse of the C-bit. CP1 is therefore 1 for protected material (e.g. pre-recorded DCC) and 0 for unprotected material.
- CP2 (copy bit 2) gives the type of digital source. CP2 = "1" for original material (pre-recorded DCC or original recordings), but = "0" for home copies. Therefore, CP2 always = "0", except for recordings from analog sources, or if the category code = 0000000 (general).
- TR0 (transparent bit 0) has the same value as CP1.
- TR1 (transparent bit 1) reserved for future use.

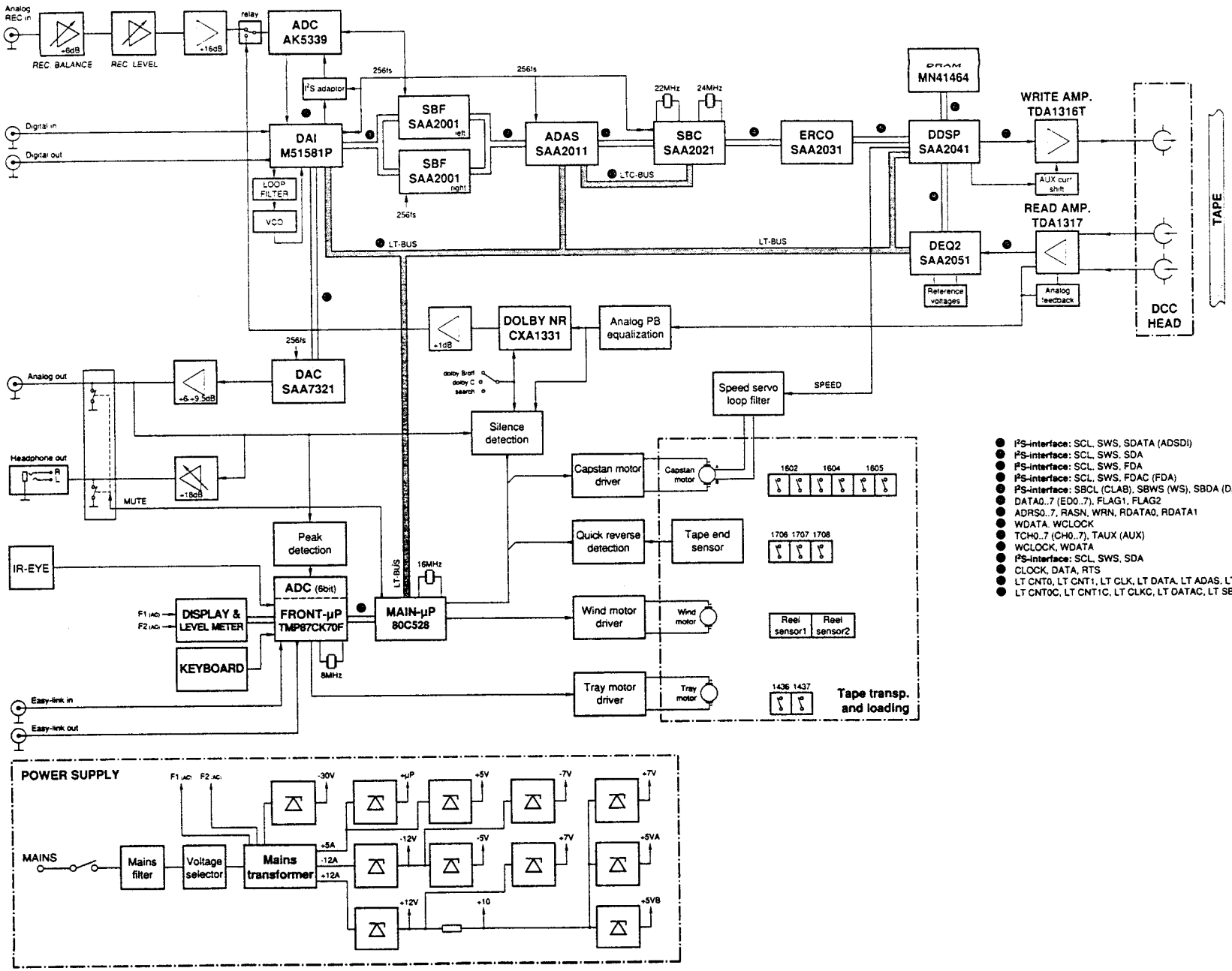
Codes CP1 and CP2 are stored in the sysinfo channel (SI0), TR0 and TR1 in the coded audio data.

CHANGE OF C- AND L-BITS ACCORDING TO IEC958

SOURCE INPUT			ON FIRST TAPE	OUTPUT AT P.B.	ON SECOND TAPE	OUTPUT AT P.B.	ON THIRD TAPE	
0000000	General	C=1 (not prot.)	CP1=1 (protected)	C=0	CP1=1	C=0	NO FURTHER	
01100xx	Act. A/D conv.	L=1 (original)	CP2=1 (prerec.)	L=1	CP2=0	L=0	RECORDING	
100xxxx	Laser opt.prod.							
010xxxx	D/D converters							
110xxxx	Magn.prod.							
001xxxx	Dig. Broadcast	C=1 (not prot.)	CP1=0 (not prot.)	C=1**	CP1=0	C=1**	CP1=0	FURTHER REC.
101xxxx	Musik instr.	L=1 (original)	CP2=0 (cons. rec.)	L=0	CP2=0	L=0	CP2=0	POSSIBLE
01101xx	Fut. A/D conv							
0001xxx	Sol state rec.							
0000001	Experimental							
0000000	General	C=1 (not prot.)	CP1=1 (protected)	C=0	CP1=1	C=0	NO FURTHER	
01100xx	Act. A/D conv.	L=0 (home copy)	CP2=1 (prerec.)	L=1	CP2=0	L=0	RECORDING	
100xxxx	Laser opt.prod.							
010xxxx	D/D converters							
110xxxx	Magn. prod.							
001xxxx	Dig. Broadcast	C=1 (not prot.)	CP1=0 (not prot.)	C=1**	CP1=0	C=1**	CP1=0	FURTHER REC.
101xxxx	Musik instr.	L=0 (home copy)	CP2=0 (cons. rec.)	L=0	CP2=0	L=0	CP2=0	POSSIBLE
01101xx	Fut. A/D conv.							
0001xxx	Sol state rec.							
0000001	Experimental							
010xxxx	D/D converters							
110xxxx	Magn. prod.							
101xxxx	Musik instr.	C=0 (protected)	NO RECORDING					
01101xx	Fut. A/D conv.	L=0 (home copy)						
0001xxx	Sol state rec.							
0000001	Experimental							
010xxxx	D/D converters							
110xxxx	Magn. prod.							
101xxxx	Musik instr.	C=0 (protected)	CP1=1 (protected)	C=0	NO FURTHER			WHITE LIST
01101xx	Fut. A/D conv.	L=1 (original)	CP2=0 (cons. rec.)	L=0	RECORDING			
0001xxx	Sol state rec.							
0000001	Experimental							
100xxxx	Laser opt. prod.	C=0 (protected)	CP1=1 (protected)	C=0	NO FURTHER			
001xxxx	Dig. Broadcast	L=0 (home copy)	CP2=0 (cons. rec.)	L=0	RECORDING			WHITE LIST
0111xxx	Dig. Broadcast							
100xxxx	Laser opt. prod.	C=alternates / L=0	NO RECORDING					
Professional		bit 0=1	NO RECORDING					
Non Audio		bit 1=1	NO RECORDING					
No category code		L or C independent	CP1=1 (protected)	C=0	NO RECORDING			
			CP2=0 (cons. rec.)	L=0				
Prerecorded DCC tape			CP1=1 (protected)	C=0	CP1=1	C=0	NO FURTHER	
			CP2=1 (original)	L=0	CP2=0	L=0	RECORDING	
Prerecorded DCC tape			CP1=1 (protected)	C=1**	CP1=0	C=1**	CP1=0	FURTHER REC.
			CP2=0 (cons. rec.)	L=0	CP2=0	L=0	CP2=0	POSSIBLE

** REMARK: if TR0=1 and CP1=0 the C-bit=0

BLOCKDIAGRAM



- I²S-interface: SCL, SWS, SDATA (ADSDI)
- I²S-interface: SCL, SWS, SDA
- I²S-interface: SCL, SWS, FDA
- I²S-interface: SCL, SWS, FDAC (FDA)
- I²S-interface: SBCL (CLAB), SBWS (WS), SBDA (DAAB), SBEF (EFAB)
- DATA0..7 (ED0..7), FLAG1, FLAG2
- ADRS0..7, RASN, WRN, RDATA0, RDATA1
- WDATA, WCLOCK
- TCH0..7 (CH0..7), TAUX (AUX)
- WCLOCK, WDATA
- I²S-interface: SCL, SWS, SDA
- CLOCK, DATA, RTS
- LT CNT0, LT CNT1, LT CLK, LT DATA, LT ADAS, LT DAI, LT DEQ, LT DDSP
- LT CNT0C, LT CNT1C, LT CLKC, LT DATAC, LT SBC

11. NOTES ON THE BLOCK DIAGRAM

There are four basically different operating modes:

– DATA PLAYBACK, AUX PLAYBACK

The head signals are first fed to the read amplifier (TDA1317), where they are amplified, filtered and supplied to a multiplexer. The output signal of the multiplexer (RDMUX) contains the information of the 8 main data tracks, the AUX channel and a dummy channel, and is passed on to the DEQ2 (SAA2051). The DEQ2 reconstructs the original digital head signals, and sends them in parallel form to the DDSP (SAA2041). This IC, together with the ERCO (SAA2031) and the DRAM (MN41464), is responsible for decoding the PASC data. System information goes to the main microprocessor via the LT-interface of the DDSP, and the coded audio data is transferred to the SBC (SAA2021) via the I²S-interface of the ERCO. In the SBC, the subband samples are computed, and they are passed on to the ADAS (SAA2011) via the I²S-interface, and from there to the two SBFs (SAA2001). The ADAS is inactive in this operating mode, so its I²S-interfaces are completely transparent. The two SBFs combine the subband samples into one audio broadband signal, and it is transferred via two more I²S-interfaces to the DAI (M51581P), and in parallel to the DAC (SAA7321). The DAI, together with system information of the main microprocessor, generates an EBU signal, which is output via DIGITAL OUT. The D/A converted audio data goes to the appropriate analog outputs via buffer amplifiers.

– DATA RECORD, AUX RECORD

In this operating mode, the audio data either reaches the DAI directly via DIGITAL IN (digital source), or is first digitized by the ADC (AK5339) (analog source). Since the ADC which is used does not support I²S-format, the interface of the ADC must be adapted to that of the DAI (I²S-adapter). The DAI passes the digital audio data on to the two SBFs via its I²S-interface. Here, the broadband signal is separated into 32 subbands. The subband samples are transferred to the ADAS via two more I²S-interfaces, for calculation of the allocation information. The subband samples themselves are not modified by the ADAS, but only passed on to the SBC with a delay (I²S-interface). The calculated allocation information is transmitted, in parallel to the (delayed) subband samples, via a dedicated LTC bus. In the SBC, the sample is scaled. The PASC data is then transferred to the ERCO, which together with the DDSP and the DRAM carries out the error coding, formation of tape frames and channel coding (ETM). The sysinfo data goes to the DDSP via the LT-interface of the main microprocessor. Finally, the tape frame data is passed on serially to the write amplifier (TDA1316T), which drives the write heads accordingly. An additional circuit block raises the writing current for the AUX channel.

– DATA PLAYBACK, AUX RECORD

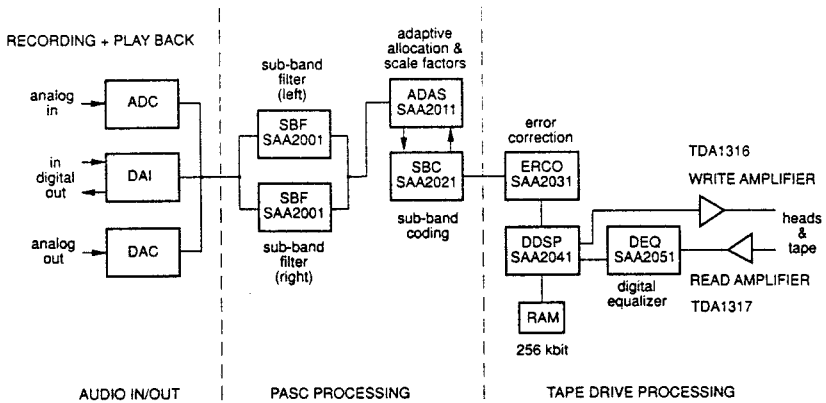
This operating mode is a combination of the modes described above, and is used for (subsequent) deletion or writing of markers on the AUX track. The DDSP continuously sends sysinfo data to the main microprocessor, and simultaneously generates AUX tape frames (together with ERCO and DRAM). The AUX data is transferred to the DDSP via the LT-interface of the main microprocessor. The tape frames generated by the DDSP are taken in serial form via WDATA to the write amplifier, which drives the AUX write head accordingly.

– CC PLAYBACK

The analog head signals are first amplified by the read amplifier, and linearised by a magnetic feedback loop. A further filter stage ensures an ideal frequency response. The analog signal is then fed to the Dolby circuit, and any distortion is corrected. The audio signal then goes via an amplifier stage to the ADC, where it is digitized. The DAI generates (with the main microprocessor) an EBU signal, which is output via DIGITAL OUT. The digital audio data is passed on to the DAC via the I²S-interface of the DAI, D/A converted, and taken to the appropriate analog outputs via buffer amplifiers.

12. DCC ICs FOR PASC

NAME	TYPE No.	PACKAGE	BODY	PINPITCH	COMPLEXITY
SBF	SAA2001	QFP44	14x14mm	1,0mm	140k transist.
ADAS	SAA2011	QFP44	14x14mm	1,0mm	268k transist.
SBC	SAA2021	QFP44	14x14mm	1,0mm	215k transist.
ERCO	SAA2031	QFP44	14x14mm	1,0mm	58k transist.
DDSP	SAA2041	QFP80	14x20mm	0,8mm	60k transist.
DEQ2	SAA2051	QFP44	14x14mm	1,0mm	51k transist.



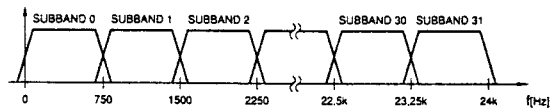
12.1. SAA2001 - subband filter for PASC coding/decoding

The task of the subband filter (SBF) is to separate digital audio input signals into 32 subbands (recording), or convert the 32 subbands back into an audio broadband signal (playback).

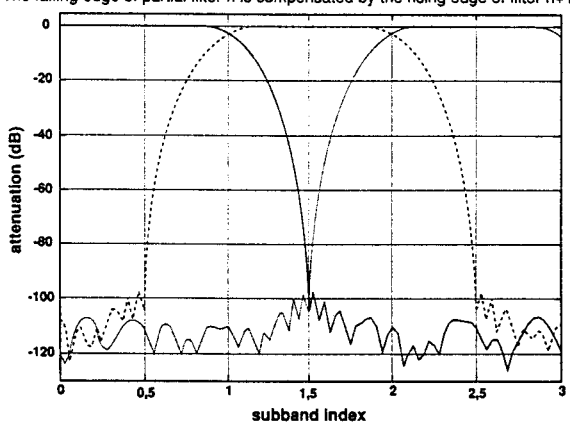
The sampling frequency of each subband is fs/32, and the corresponding bandwidth is fs/64. Therefore:

fs BROADBAND	fs SUBBAND	BANDWIDTH
48kHz	1500Hz	750Hz
44,1kHz	1378Hz	689Hz
32kHz	1000Hz	500Hz

For a stereo (or 2-channel mono) PASC system, two SBFs are required. The filter bank is implemented as a QMF (quadrature mirror filter) in FIR technology (pulse response 512 samples), and shows linear frequency and phase response over the total transmission range.

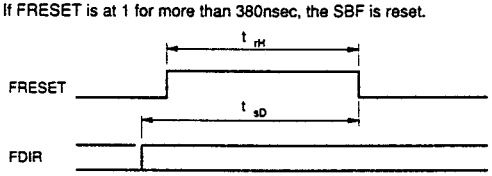


The falling edge of partial filter n is compensated by the rising edge of filter n+1.



12.1.1. FRESET RESET LINE

If FRESET is at 1 for more than 380nsec, the SBF is reset.

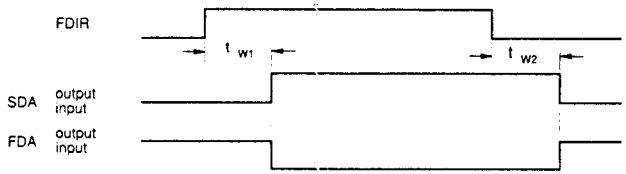


$t_{rH} \geq 380$ ns minimum time FRESET HIGH

$t_{sD} \geq 380$ ns minimum set-up time FDIR to FRESET = LOW

12.1.2. SBF OPERATING MODES

The operating mode of the SBF is determined by the FDIR control line. FDIR = "0" means code mode (recording), FDIR = "1" means decode mode (playback).

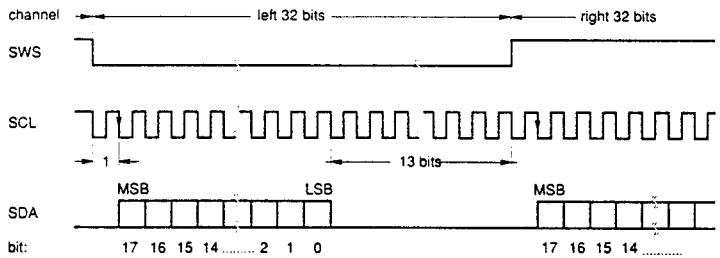


$t_{w1} \geq 380$ ns minimum time before FDA enabled

$t_{w2} \geq 380$ ns minimum time before FDA enabled

12.1.3. TRANSMISSION OF AUDIO BROADBAND SAMPLES

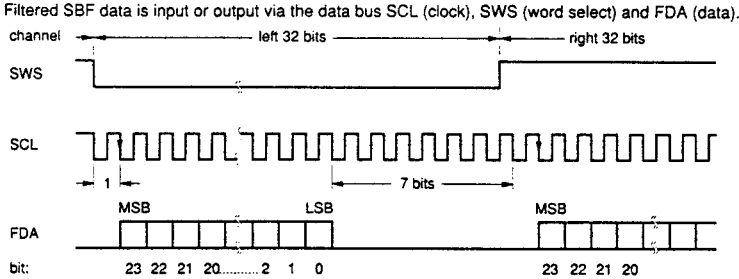
Audio broadband samples are input or output via the data bus SCL (clock), SWS (word select) and SDA (data), (bidirectional).



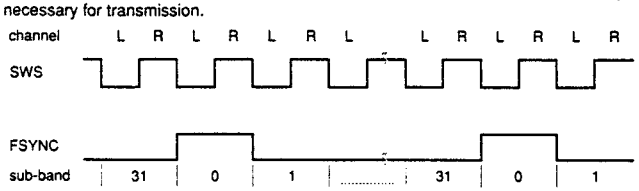
The SWS signal is "0" when data of the left channel is transmitted, and "1" for the right channel. Its frequency is the sampling frequency fs. The clock frequency at SCL is 64 times the sampling frequency.

12.1.4. TRANSMISSION OF SUBBAND SAMPLES

Filtered SBF data is input or output via the data bus SCL (clock), SWS (word select) and FDA (data).



Because no unique assignment of subband data to the appropriate filter bank is possible, the additional data line FSYNC is necessary for transmission.



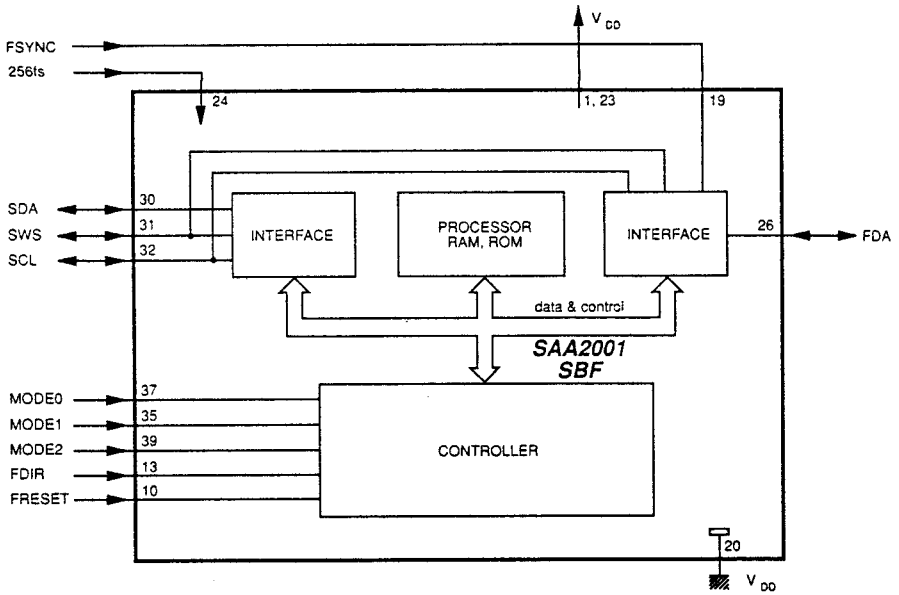
This signal is "1" when data of subband 0 is being transmitted. The frequency of FSYNC is 1/32 of the sampling frequency fs.

12.1.5. MODE SELECTION CONTROL LINES

Three control lines (MODE0, MODE1 amd MODE2) per SBF define the data channel (left or right) and the interface mode of the broadband signal.

MODE0	MODE1	MODE2	INTERFACE MODE	CHANNEL
0	0	0	I2S-Interface mode	left channel
0	0	1	I2S-Interface mode	right channel
0	1	x	not used for PASC	
1	0	x	not used for PASC	
1	1	x	not used for PASC	

12.1.6. BLOCK DIAGRAM AND PIN CONFIGURATION



1	VDD	positive supply voltage (+5V)
2	TEST1	do not connect
3	n.c.	not connected
4	TEST2	do not connect
5	n.c.	not connected
6	TEST3	do not connect
7	n.c.	not connected
8	TEST4	do not connect
9	n.c.	not connected
10	FRESET	input reset signal from SBC (SAA2021)
11	n.c.	not connected
12	n.c.	not connected
13	FDIR	filtered I²S-interface direction control input
14	TEST5	test input; to be connected to Vss
15	TEST6	do not connect
16	n.c.	not connected
17	TEST7	test input; to be connected to Vss
18	n.c.	not connected
19	FSYNC	sub-band synchronization on filtered I2S-interface input
20	Vss	supply ground (0V)
21	TEST8	do not connect
22	n.c.	not connected
23	VDD	positive supply voltage (+5V)
24	256fs	system clock input; 256 x sample frequency
25	n.c.	not connected
26	FDA	I/O filtered data; I²S-interface (3-state inputs/outputs)
27	n.c.	not connected
28	n.c.	not connected
29	n.c.	not connected
30	SDA	I/O data; I²S-interface (3-state inputs/outputs)
31	SWS	word selection input; (filtered) I²S-interface
32	SCL	bit-clock input; (filtered) I²S-interface
33	n.c.	not connected
34	n.c.	not connected
35	MODE1	operation mode selection 1 input
36	n.c.	not connected
37	MODE0	operation mode selection 0 input
38	n.c.	not connected
39	MODE2	operation mode selection 2 input
40	n.c.	not connected
41	n.c.	not connected
42	n.c.	not connected
43	Vss	supply ground (0V)
44	n.c.	not connected

12.2. SAA2011 - ADAPTIVE ALLOCATION AND SCALING

Tasks of the ADAS during recording:
In encoding mode (FDIR = "0"), the subband samples of a PASC frame are first transferred from the two SBFs to the ADAS. From these 2 x 12 x 32 samples, the ADAS calculates the allocation information, that is the height of the quantisation for each subband. The subband samples are then passed on to the SBC, together with the allocation information. The subband samples are not modified by the ADAS. but passed on to the SBC unchanged (but delayed). The ADAS continuously monitors the status of the SBC (bit rate, sampling frequency, emphasis), and begins the data transfer after receiving the "ready to receive bit".

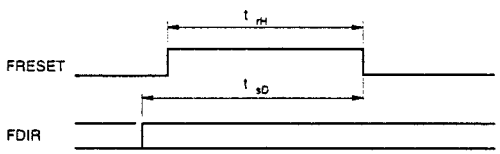
Tasks of the ADAS during playback:
In decoding mode (FDIR = "1"), the ADAS receives subband samples from the SBC. and passes them on to the SBF unchanged after 160 SWS cycles.

Because the SBC does not have its own LT-interface, the µP and SBC exchange data via the ADAS, synchronously with the SBC operations:
- At each FSYNC, the ADAS reads the status of the SBC.
- After each calculation of the allocation information, the ADAS sends the first 16-bit allocation unit.The status of the SBC is then read until it is ready to receive the next data. After receiving "ready to receive" from the SBC, the ADAS sends the next unit, followed by settings.
- External settings sent by the microprocessor are passed on to the SBC as soon as possible.

The microprocessor communicates with the ADAS in a similar way:
- The status of the ADAS can be read continuously by the microprocessor.
- Settings can be sent after each positive edge of the "ready to receive bit S".
- External settings can be sent after each positive edge of the "ready to receive bit E".

12.2.1. RESET AND POWER DOWN

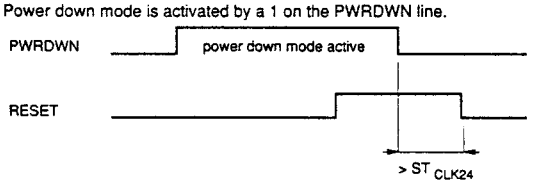
If FRESET is at 1 for more than 210nsec, the ADAS is reset and is then in playback mode.



$t_{rH} \geq 210$ ns minimum time FRESET HIGH

$t_{SD} < 0$ ns minimum set-up time FDIR to FRESET = LOW

Power down mode is activated by a 1 on the PWRDWN line.

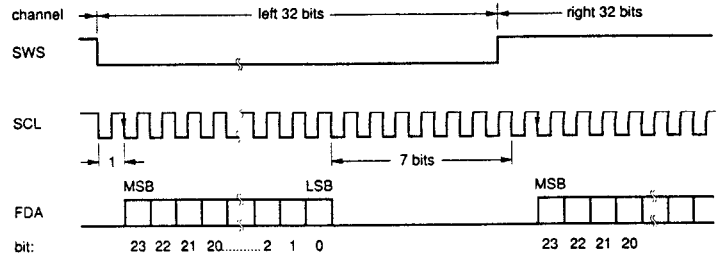


12.2.2. ADAS OPERATING MODES

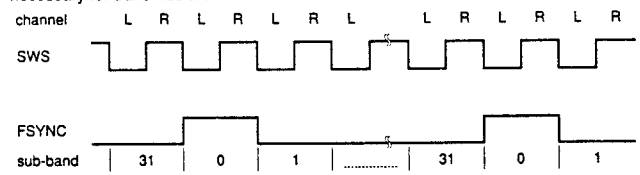
The operating mode of the ADAS is determined by the FDIR control line. FDIR = "0" means code mode (recording), FDIR = "1" means decode mode (playback).

12.2.3. TRANSMISSION OF SUBBAND DATA TO AND FROM SBF

The filtered SBF data is input or output via the data bus SCL (clock), SWS (word select) and FDAF (data) (bidirectional).



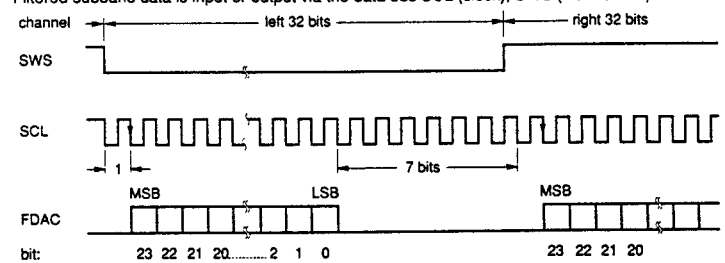
Because no unique assignment of subband data to the appropriate filter bank is possible, the additional data line FSYNC is necessary for transmission.



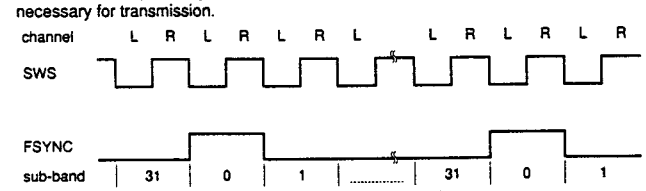
This signal is "1" when data of subband 0 is being transmitted. The frequency of FSYNC is 1/32 of the sampling frequency fs.

12.2.4. TRANSMISSION OF SUBBAND DATA TO AND FROM SBC

Filtered subband data is input or output via the data bus SCL (clock), SWS (word select) and FDAC (data).



Because no unique assignment of subband data to the appropriate filter bank is possible, the additional data line FSYNC is necessary for transmission.



This signal is "1" when data of subband 0 is being transmitted. The frequency of FSYNC is 1/32 of the sampling frequency fs.

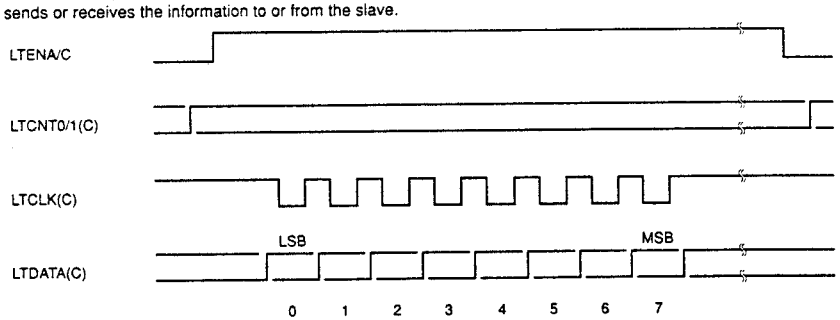
12.2.5. LT-INTERFACES

The ADAS is equipped with two LT-interfaces. One interface is responsible for exchanging data between the ADAS and the SBC, the other for data transmission between the ADAS and the microprocessor. Which information is transferred is determined by the control lines LTCNT0 and LTCNT1:

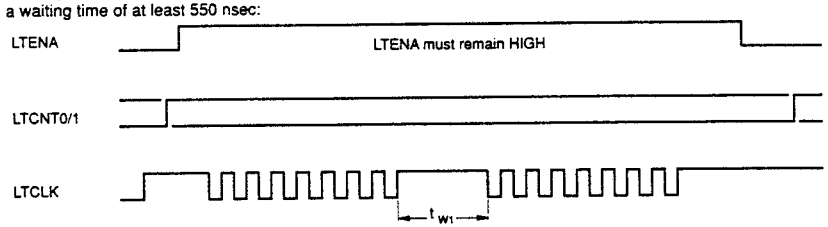
LTCNT1(C)	LTCNT0(C)	MODE	FROM	TO	TRANSFER OF
0	0	External settings	µP	SBC	8bits
0	1	Allocation info*	ADAS	SBC	2x32x4bits
1	0	Settings	µP	SBC	16bits
1	1	Status	SBC	µP	8 or 16bits

* This mode is only possible on the ADAS ↔ SBC interface.

Before each data transmission, the master first determines the mode (control lines LTCNT0(C) and LTCNT1(C). LTENA(C) is then set to "1", and the selected mode is activated by the positive edge. The master then provides the clock (LTCLK(C)), and sends or receives the information to or from the slave.

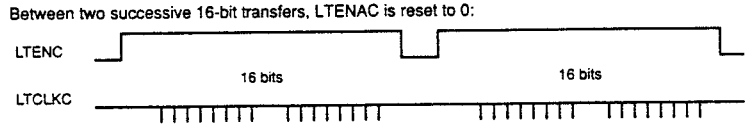


The data words transferred always have a length of 8 or 16 bits, the 16 bits being divided into two units of 8 bits each. The LSB is always the first bit sent. If there are two units, the most significant unit is sent first. Between two blocks of 8 bits, there must be a waiting time of at least 550 nsec:



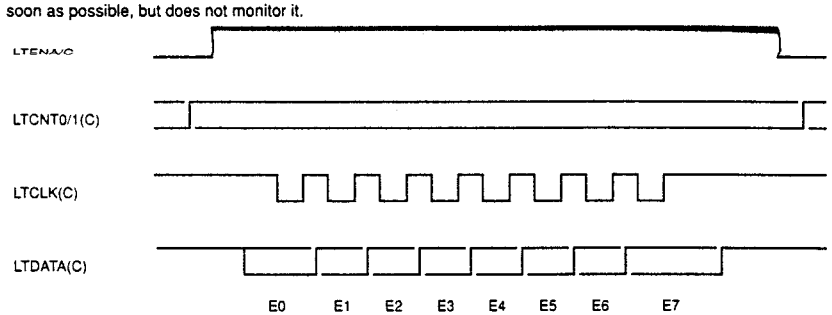
$t_{w1} \geq 550$ ns minimum time between two 8-bit transfers

Between two successive 16-bit transfers, LTENAC is reset to 0:



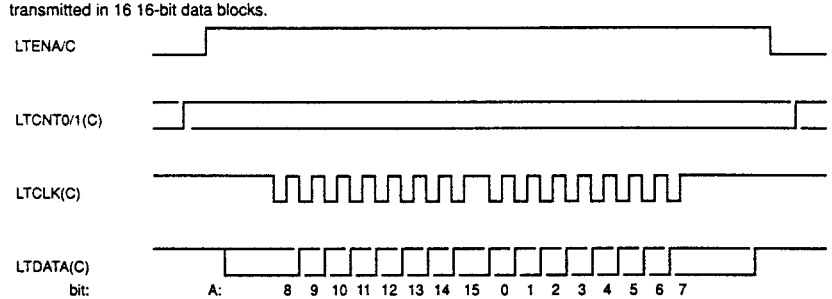
12.2.6. TRANSMISSION OF EXTERNAL SETTINGS (LTCNT1(C) = "0", LTCNT0(C) = "0")

This data consists of 8 information bits from the microprocessor to the ADAS. The ADAS passes this data on to the SBC as soon as possible, but does not monitor it.



12.2.7. TRANSMISSION OF ALLOCATION INFORMATION (LTCNT1C = "0", LTCNT0C = "1")

The allocation information (4 bits per subband) is transmitted once per subband frame, in recording mode only (FDIR = "0"). The 4 bits of information give the number of bits - 1 assigned to the subband. The value 0000 means that in the corresponding subband no data is coded. The 2 x 32 x 4 bits (2 channels, 32 subbands) of allocation information per subband frame are transmitted in 16 16-bit data blocks.



The 16 allocation bits of one data block have the following meaning:

Bits	Channel	Allocation-Info for Subband
A15..A12	L (I)	0, 2, 4, 8, ..., 30
A11..A8	R (II)	0, 2, 4, 8, ..., 30
A7..A4	L (I)	1, 3, 5, 7, ..., 31
A3..A0	R (II)	1, 3, 5, 7, ..., 31

After each data word is sent, the ADAS waits for the ready to receive bit of the SBC. The LTENAC line is meanwhile 0. After successful transmission, settings are sent again. These 16-bit words have the following meanings:

Bit(s)	Name	Meaning	Mode
S15..S12	Bitrate Index	Bitrate Indication	recording
S11..S10	Sampling frequency	32, 44,1 oder 48kHz	recording
S9	DECODE		rec./playback
S8	ext. 256fs	"1"-ext., "0"-int.	recording
S7	2-ch. mono	"1"-2 ch. mono, "0"-stereo	recording
S6	MUTESBF	"1"-mute, "0"-no mute	rec./playback
S5	IDLE	"1"-idle, "0"-not idle	rec./playback
S4	CH I	"1"-ch. I, "0"-ch. II	playback
S3..S2	TR1-TR0	Transparent bits	recording
S1..S0	EMPHASIS	Emph. Indication	recording

12.2.8. INTERROGATING THE STATUS WORD (LTCNT1(C) = "1", LTCNT0(C) = "1")

The status of the ADAS and SBC can be continuously monitored by interrogating the status word. This word is 16 bits long and has the following meaning:

T15..T12: bit rate index
indicates the bit rate of the subband signal in units of 32 kbit/sec (ADAS: 384 kbit/sec)
T11..T10: sampling frequency indication, defined as follows:

MSB	LSB	SAMPLING FREQU.
0	0	44,1kHz
0	1	48kHz
1	0	32kHz
1	1	not used

T9: ready to receive bit S
T8: ready to receive bit E

These bits indicate whether the ADAS is ready to receive new settings (S) or external settings (E). (Ready = "1" for either S or E.) These bits are interrogated each time before new information is sent.

T7..T6: MODE
The mode bits have the following meaning:

MSB	LSB	MODE	OUTPUT
0	0	stereo	L and R
0	1	–	reserved
1	0	2-channel mono	I or II as selected
1	1	–	reserved

T5: SYNC
In recording mode, this bit is used for synchronisation (see SBC).

In playback mode, this bit indicates whether the operations of the SBC are synchronous with the subband signal. If this is not the case, correct decoding is not possible.

T4: CLKOK
indicates whether the specified sampling frequency agrees with the clock frequency (256fs). (OK = "1".)
T3..T2: TR1, TR0
These two bits indicate the copy status of the recording (see also 10. "SCMS").

T1..T0: EMPHASIS
This bit is set for emphasis recordings (15/50sec), and causes the allocation calculated by ADAS to be corrected. (The signal power of the subbands must be adapted to the transmission function.)

The ready to receive bits are generated by the ADAS. All other bits of the status word are generated by the SBC.

12.2.9. SELECTION OF THE QUANTISATION OF THE SBF DATA USED IN CALCULATING THE ALLOCATION

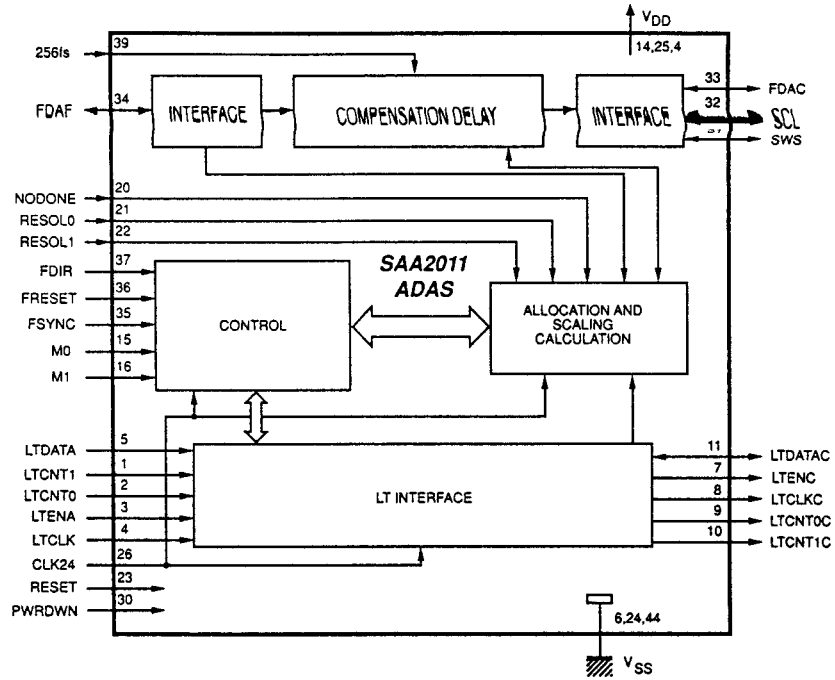
The internal resolution of the ADAS can be set externally via control lines RESOL0 and RESOL1:

RESOL0	RESOL1	RESOLUTION
0	0	16bit
0	1	18bit
1	0	14bit
1	1	15bit

12.2.10. RECORDING SIGNALS BELOW THE CALCULATED HEARING THRESHOLD

In principle, if the signal power of a subband is below the hearing threshold, it is not coded. Therefore, musical items or passages with low spectral distribution do not use much of the available storage capacity. If the control line NODONE is set to "1", the remaining bits are used to code these masked subbands. However, this simultaneously makes the values of THD and SNR worse (more signals on the tape), so that in practice this operating mode should not be used.

12.2.11. BLOCK DIAGRAM AND PIN CONFIGURATION

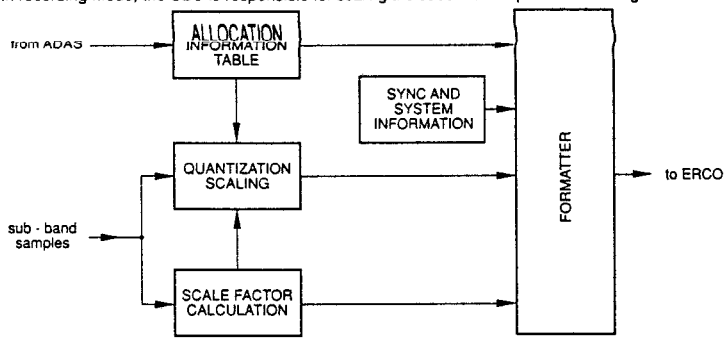


1	LTCNT1	mode control1, microcontroller interface input
2	LTCNT0	mode control0, microcontroller interface input
3	LTENA	enable microcontroller interface input
4	LTCLK	bit-clock microcontroller interface input
5	LTDATA	data, microcontroller interface (3-state inputs/outputs)
6	Vss	supply ground
7	LTCNT1C	control1; microcomputer interface, SBC (SAA2021) side output
8	LTCNT0C	control0; microcomputer interface, SBC (SAA2021) side output
9	LTENC	enable microcontroller interface, SBC (SAA2021) side output
10	LTCLKC	bit-clock; microcontroller interface, SBC (SAA2021) side output
11	LTDATAC	data; microcontroller interface, SBC (SAA2021) side output
12	TEST1	test output; do not connect
13	TEST2	test output; do not connect
14	VDD	positive supply voltage (+5V)
15	TEST3	test mode input; to be connected to VDD
16	TEST4	test mode input; to be connected to VDD
17	TEST5	test input; to be connected to Vss
18	TEST6	test input; to be connected to Vss
19	TEST7	test input; to be connected to Vss
20	NODONE	no done; state selection input
21	RESOL0	resolution; selection0 input
22	RESOL1	resolution; selection1 input
23	RESET	active HIGH reset input
24	VDD	positive supply voltage (+5V)
25	Vss	suply ground (0V)
26	CLK24	24,576MHz processing clock input
27	TEST8	test input; to be connected to Vss
28	TEST9	test input; to be connected to Vss
29	TEST10	test input; to be connected to Vss
30	PWRDWN	power-down input
31	SWS	word selection input; filtered-I²S-interface
32	SCL	bit-clock input; filtered-I²S-interface
33	FDAC	filtered data filtered-I²S-interface; SBC (SAA2021) side (3-state inputs/outputs)

34	FDAF	filtered data filtered-I²S-interface; SBF (SAA2001) side (3-state inputs/outputs)
35	FSYNC	sub-band synchronization on filtered-I²S-interface, input
36	FRESET	reset signal input from SBC (SAA2011)
37	FDIR	direction of the I²S-interface; input
38	TEST11	test input6; to be connected to VDD
39	256fs	system clock input; 256 x sample frequency
40	VDD	positive supply voltage (+5V)
41	n.c.	not connected
42	n.c.	not connected
43	n.c.	not connected
44	Vss	supply ground (0V)

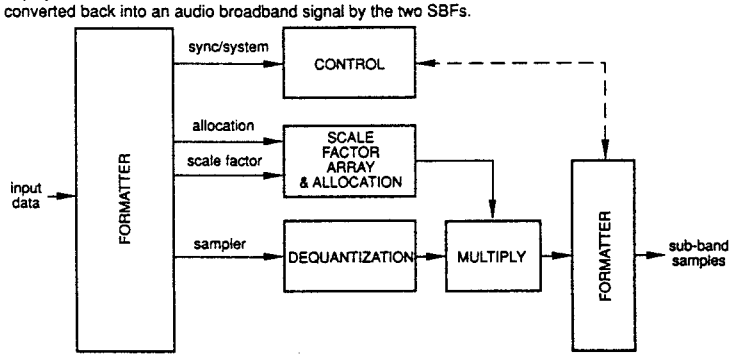
12.3. SAA2021 - Subband encoder/decoder

Tasks of the SBC during recording:
In recording mode, the SBC is responsible for scaling the subband samples and forming the PASC frames for the ERCO.



For each frame, 2 x 12 x 32 subband samples and 32 x 4 bits of allocation information are sent to the SBC by the ADAS.

Tasks of the SBC during playback:
In playback mode, the SBC receives PASC frames from the ERCO and uses these to reconstruct subband samples, which are converted back into an audio broadband signal by the two SBFs.



Special functions:
- URDA = "1" prevents decoding of invalid data, and causes a "soft mute" of the SBC data output.
- SYNCDAI is for synchronisation of an external source with fs256.
- IDLE switches the activities of the SBC to a standby state.

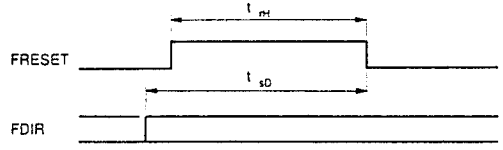
12.3.1. QUARTZ OSCILLATORS

The SBC is fitted with two quartz oscillators, 24,576 and 22,5792MHz. All clock signals required by the DCC system are derived from these frequencies.

12.3.2. RESET LINE RESET

Every falling edge on the RESET line causes the SBC to be reset to its default values.

12.3.3. RESET LINE FRESET



$t_{rH} \geq x$ ns minimum time FRESET HIGH

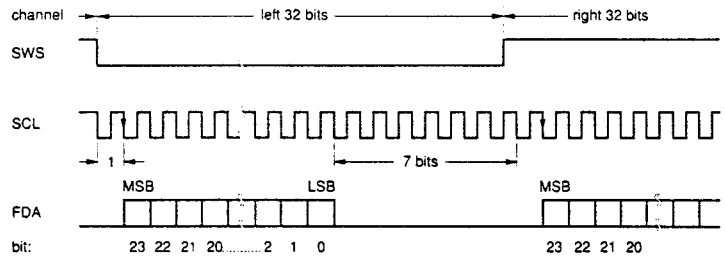
$t_{SD} \geq x$ ns minimum set-up time FDIR to FRESET = LOW

12.3.4. OPERATING MODES OF THE SBC

The operating mode of the SBC is determined by the FDIR control line. FDIR = "0" means code mode (recording), FDIR = "1" means decode mode (playback).

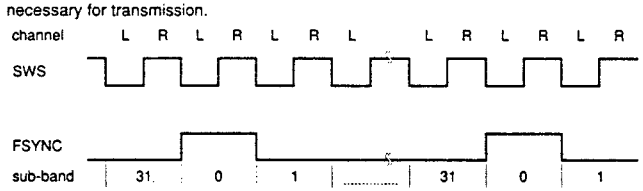
12.3.5. TRANSMISSION OF SUBBAND DATA TO AND FROM ADAS

Filtered SBF data is input or output via the data bus SCL (clock), SWS (word select) and FDA (data).



Clocked SCL is at 64fs. SWS at fs.

Because no unique assignment of subband data to the appropriate filter bank is possible, the additional data line FSYNC is necessary for transmission.

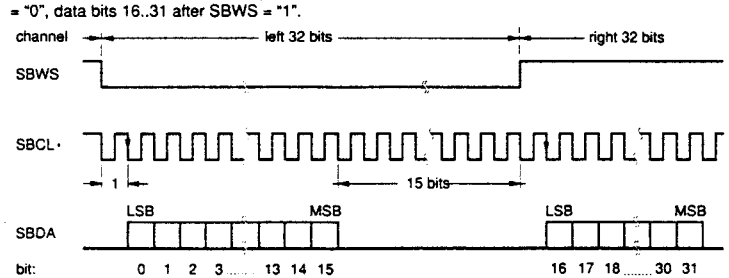


This signal is "1" when data of subband 0 is being transmitted. The frequency of FSYNC is 1/32 of the sampling frequency fs.

12.3.6. PASC CODED INTERFACE TO AND FROM ERCO

PASC data is transferred between SBC and ERCO via the data lines SBCL (clock), SBWS (word select), SBDA (data), and the control line SBEF (error signal).

64 bits are transferred with each cycle of SBWS, of which 32 are the true PASC data. Data bits 0..15 are transferred after SBWS = "0", data bits 16..31 after SBWS = "1".



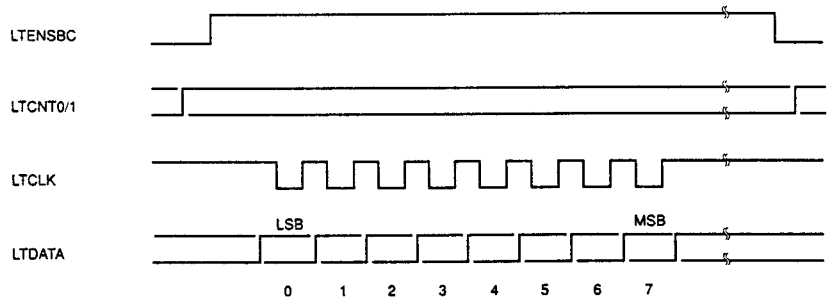
In code mode the system clock (256fs) has to be reconstructed from the EBU-signal of the external digital source (see also 12.9.6). The DDSP works with a master frequency of 24,576MHz, which is transmitted by the SBC via CLK24. Deviations between regenerated master clock and internal clock reference (quartz) are compensated by the IFG (see also 7.3). In record mode the value of the error signal SBEF is meaningless and can be ignored.
In decode mode SBCL and SBWS are generated by the SBC. The error signal SBEF gives the error status of bytes being transferred. SBEF = "1" indicates an uncorrectable error in the data word transmitted.

12.3.7. CONTROL LINES FROM THE DDSP TO THE SBC

The control lines SBDIR (data transfer direction) and URDA (unreliable coded data signal) complete the I²S-interface from the ERCO to the SBC.
SBDIR gives the direction of data transfer between ERCO and SBC, and is "1" for playback.
URDA = "1" indicates an erroneous data transfer, independently of all other flag information. This applies to main, sysinfo and AUX data. URDA occurs when the operating mode changes from recording to playback, or if the DDSP has to be resynchronised with the tape signals.

12.3.8. LT-INTERFACE

The SBC is equipped with an LT-interface, which enables data to be transferred between the ADAS and SBC. The ADAS is the master. The interface consists of the data lines LTCLK (clock), LTDATA (data) and LTENSBC (enable), and the control lines LTCNT0 and LTCNT1.

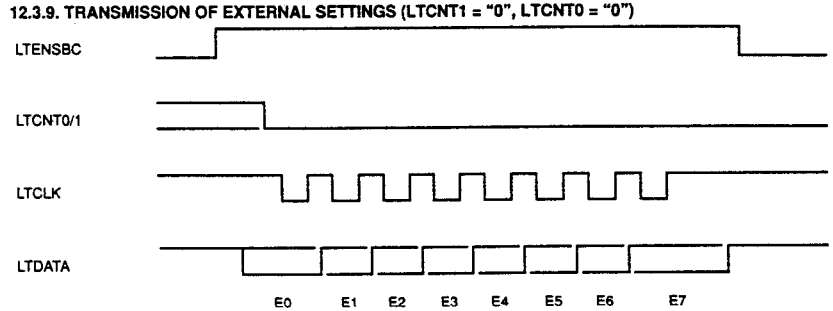


LTCNT0 and LTCNT1 give the type of data:

LTCNT1	LTCNT0	MODE	FROM	TO	TRANSFER OF
0	0	External settings	ADAS	SBC	8bits
0	1	Allocation	ADAS	SBC	2x32x4bits
1	0	Settings	ADAS	SBC	16bits
1	1	Status	SBC	ADAS	8 or 16bits

Before each data transmission, the master first determines the mode (control lines LTCNT0 and LTCNT1). LTENSBC is then set to "1", and the selected mode is activated by the positive edge. The master then provides the clock (LTCLK), and sends or receives the information to or from the slave. Data words with a length of 8 or 16 bits are transferred, the 16 bits being divided into two units of 8 bits each. The LSB is always the first bit sent. If there are two units, the most significant unit is sent first.

12.3.9. TRANSMISSION OF EXTERNAL SETTINGS (LTCNT1 = "0", LTCNT0 = "0")



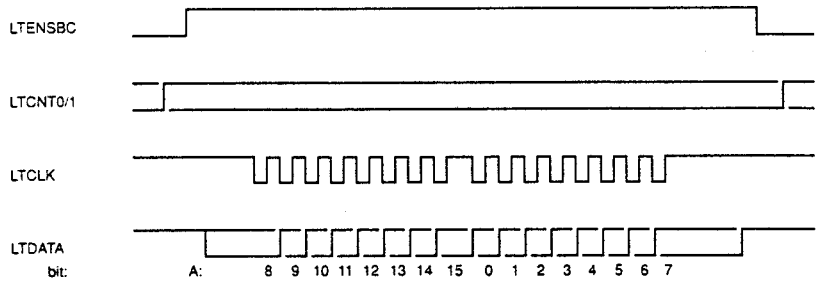
This data consists of 8 information bits from the ADAS to the SBC, with the following meaning:

BIT	NAME	DESCRIPTION	DEFAULT
E0	MUTEDAC	Connected to DAC mute input	1
E1	ATTDAC	Connected to DAC attenuation input	0
E2	DEEMDAC	Emphasis control	0
E3	HOLDCLKOK	Selects the mode of CLOCKOK indication	0
E4..E7	"don't care"	Bits will be transfered regardless	

Die bits E0..E2 are copied directly to the corresponding outputs after the 8 information bits are received.
Bit E3 specifies the mode in which CLKOK is updated:
E3 = "1" - when CLKOK becomes 0, this state is retained until new settings are received ("Hold-Mode").
E3 = "0" - the current value of fs is continuously compared with the expected value of fs, and the result is in CLKOK ("Follow-Mode").

12.3.10. TRANSMISSION OF ALLOCATION INFORMATION (LTCNT1 = "0", LTCNT0 = "1")

The allocation information (4 bits per subband) is transmitted every 8msec once per subband frame, in recording mode only (FDIR = "0"). The 4 bits of information give the number of bits - 1 assigned to the subband. The value "0000" means that in the corresponding subband no data is coded. The 2 x 32 x 4 bits (2 channels, 32 subbands) of allocation information per subband frame are transmitted in 16 16-bit data blocks.



The 16 allocation bits of one data block have the following meaning:

Bits	Channel	Allocation-Info for Subband
A15..A12	L (I)	0, 2, 4, 8, ..., 30
A11..A8	R (II)	0, 2, 4, 8, ..., 30
A7..A4	L (I)	1, 3, 5, 7, ..., 31
A3..A0	R (II)	1, 3, 5, 7, ..., 31

After each data word is sent, the ADAS waits for the ready to receive bit of the SBC. The LTENAC line is meanwhile "0". After successful transmission, settings are sent again. These 16-bit words have the following meanings:

Bit(s)	Name	Meaning	Mode
S15..S12	Bitrate Index	Bitrate Indication	recording
S11..S10	Sampling frequency	32, 44,1 oder 48kHz	recording
S9	DECODE		rec./playback
S8	ext. 256fs	"1"-ext., "0"-int.	recording
S7	2-ch. mono	"1"-2 ch. mono, "0"-stereo	recording
S6	MUTESBF	"1"-mute, "0"-no mute	rec./playback
S5	IDLE	"1"-idle, "0"-not idle	rec./playback
S4	CH I	"1"-ch. I, "0"-ch. II	playback
S3..S2	TR1-TR0	Transparent bits	recording
S1..S0	EMPHASIS	Emph. Indication	recording

12.3.11. INTERROGATING THE STATUS WORD (LTCNT1(C) = "1", LTCNT0(C) = "1")

The status of the ADAS and SBC can be continuously monitored by interrogating the status word. This word is 16 bits long, and has the following meaning:

T15..T12: bit rate index
indicates the bit rate of the subband signal in units of 32 kbit/sec (DCC: 384 kbit/sec)

T11..T10: sampling frequency indication, defined as follows:

MSB	LSB	SAMPLING FREQU.
0	0	44,1kHz
0	1	48kHz
1	0	32kHz
1	1	not used

T9: ready to receive bit S
T8: ready to receive bit E
These bits indicate whether the ADAS is ready to receive new settings (S) or external settings (E). (Ready = "1" for either S or E.) These bits are interrogated each time before new information is sent.

T7..T6: MODE
The mode bits have the following meaning:

MSB	LSB	MODE	OUTPUT
0	0	stereo	L and R
0	1	–	reserved
1	0	2-channel mono	I or II as selected
1	1	–	reserved

T5: SYNC
In recording mode, this bit is used for synchronisation (see SBC).
In playback mode, this bit indicates whether the operations of the SBC are synchronous with the subband signal. If this is not the case, correct decoding is not possible.

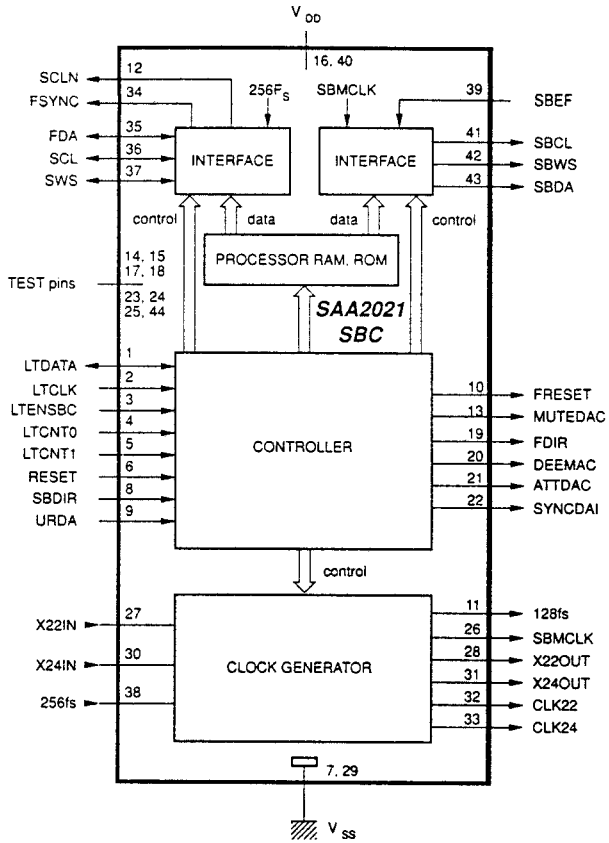
T4: CLKOK
indicates whether the specified sampling frequency agrees with the clock frequency (256fs). (OK = "1".)

T3..T2: TR1, TR0
These two bits indicate the copy status of the recording (see also 10. SCMS).

T1..T0: EMPHASIS
This bit is set for emphasis recordings (15/50sec), and causes the allocation calculated by ADAS to be corrected. (The signal power of the subbands must be adapted to the transmission function.)

The ready to receive bits are generated by the ADAS. All other bits of the status word are generated by the SBC.

12.3.12. BLOCK DIAGRAM AND PIN CONFIGURATION



1	LTDATA	data, microcontroller interface (3-state inputs/outputs)
2	LTCLK	bit-clock microcontroller interface input
3	LTENSBC	enable microcontroller interface input
4	LTCNT0	microcontroller; mode control0 input
5	LTCNT1	microcontroller; mode control1 input
6	RESET	system reset input; resets if 1
7	Vss	supply ground (0V)
8	SBDIR	I²S-interface directional control input
9	URDA	unreliable PASC coded data input
10	FRESET	reset signal output from SBF (SAA2001)
11	128fs	256fs output devided by two clock output
12	SCLN	inverted bit-clock filtered I²S-interface output
13	MUTEDAC	control output for D/A converter
14	TESTO0	test output; do not connect
15	TESTO1	test output; do not connect
16	VDD	positive supply voltage (+5V)
17	TESTI0	test input; to be connected to Vss
18	TESTI1	test input; to be connected to Vss
19	FDIR	filtered I²S-interface and SBF (SAA2001) operational control output
20	DEEMDAC	D/A converter control output
21	ATTDAC	D/A converter control output
22	SYNCDAI	external clock source synchronization output
23	TESTO2	test output; do not connect
24	TESTO3	test output; do not connect

25	TESTI2	test input; to be connected to Vss
26	SBMCLK	master clock output; 6,144MHz
27	X22IN	22,5792MHz crystal input
28	X22OUT	22,5792MHz crystal output
29	Vss	supply ground (0V)
30	X24IN	24,576MHz crystal input
31	X24OUT	24,576MHz crystal output
32	CLK22	22,5792MHz buffered output
33	CLK24	24,576MHz buffered output
34	FSYNC	filtered-I²S-interface sub-band synchronization output
35	FDA	filtered-I²S-interface filtered data (3-state inputs/outputs)
36	SCL	filtered-I²S-interface bit-clock (3-state inputs/outputs)
37	SWS	word selection; filtered-I²S-interface (3-state inputs/outputs)
38	256fs	system clock input; 256 x sample frequency (3-state inputs/outputs)
39	SBEF	error signal input for sub-band-I²S-interface
40	VDD	positive supply voltage (+5V)
41	SBCL	bit-clock I²S-interface (3-state inputs/outputs)
42	SBWS	I²S-interface word selection (3-state inputs/outputs)
43	SBDA	coded sub-band data I²S-interface (3-state inputs/outputs)
44	TESTI3	test input; connect to Vss

12.4. SAA2031 - Error correction encoder/decoder

The ERCO has three different operating modes:

– DPAP - data playback, aux playback

In this mode, the regenerated data of the 9 data tracks are demodulated by the DDSP, and stored temporarily in the DRAM. Error correction is then carried out by the ERCO, during which the DDSP controls the data flow to and from the ERCO. After a tape frame has been decoded, the PASC data is transferred to the SBC via the I²S-interface of the ERCO. The DDSP sends AUX and sysinfo data to the microprocessor via the LT-interface.

– DPAR - data playback, aux record

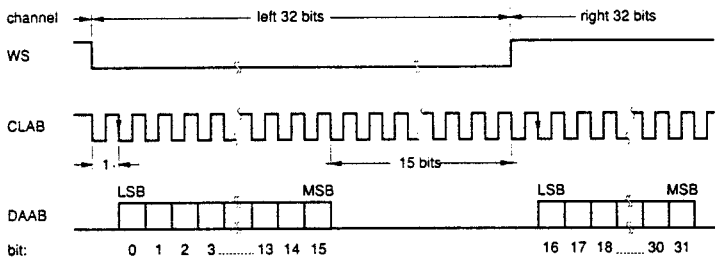
In this mode, the microprocessor writes AUX data to the DDSP, and reads sysinfo data from it. The regenerated digital signals of the 8 main data tracks are demodulated, and stored temporarily in the DRAM. Error correction is carried out with the ERCO (controlled by the DDSP). The PASC data is then transferred to the SBC via the I²S-interface of the ERCO. Simultaneously, the AUX data is formatted into a tape block, adding block headers, ETM, sync pattern and IFG.

– DRAR - data record, aux record

In this mode, PASC data is written via the I²S-interface of the ERCO to the DDSP, and then into the DRAM. AUX and sysinfo data is received from the microprocessor via the LT-interface and also stored in the DRAM. Error coding is carried out by the ERCO (controlled by the DDSP). The DDSP then forms the data in the DRAM into a tape block, adding block headers, ETM, sync pattern and IFG.

12.4.1. PASC CODED INTERFACE TO AND FROM SBC

PASC data is transferred between SBC and ERCO via the data lines CLAB (clock), WS (word select), DAAB (data), and the control line EFAB (error signal). 64 bits are transferred at each cycle of SBWS, of which 32 are the true PASC data. Data bits 0..15 are transferred after WS = "0", data bits 16..31 after WS = "1".

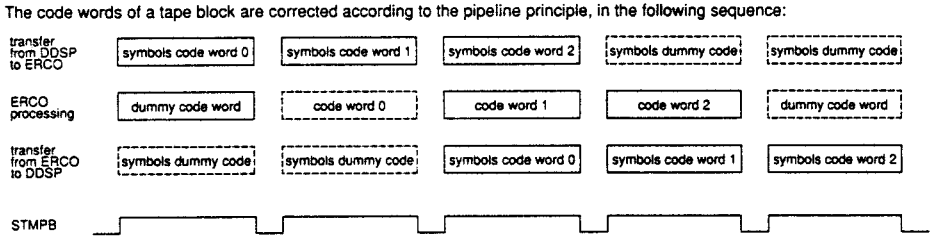


In code mode the system clock (256fs) has to be reconstructed from the EBU-signal of the external digital source (see also 12.9.6). The DDSP works with a master frequency of 24,576MHz, which is transmitted by the SBC via CLK24. Deviations between regenerated master clock and internal clock reference (quartz) are compensated by the IFG (see also 7.3). In record mode the value of the error signal EFAB is meaningless and can be ignored.
In decode mode CLAB and WS are generated by the SBC. The error signal EFAB gives the error status of bytes being transferred. EFAB = "1" indicates an uncorrectable error in the data word transmitted.

12.4.2. DATA TRANSFER BETWEEN DDSP AND ERCO

Data is transferred between DDSP and ERCO via the data bus DATA0..DATA7, the flags FLAG1 and FLAG2, and the control lines OERDCB, READB and SELERF!.

The code words of a tape block are corrected according to the pipeline principle, in the following sequence:

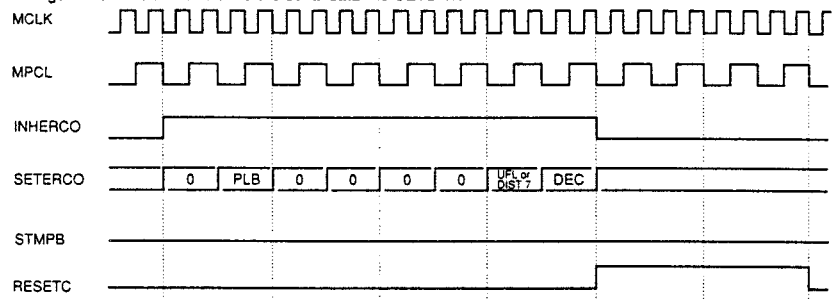


1. The DDSP sends a so-called "REceived Symbol", RES(n), to the ERCO. At this time, SELERFI = "1", OERDCB = "1", and READB = "0".
2. While RES(n) is being transferred, the ERCO corrects a previously sent code word RES(n-1).
3. A previously corrected symbol COS(n-2) is then written from the ERCO to the DDSP. At this time, OERDCB = "0".

Since no previous code word exists after the first RES of a block is transferred, the ERCO corrects a so-called "dummy symbol". The first two COSs transferred to the DDSP are therefore invalid, and are ignored by the DDSP. Similarly, at the end of the block, two dummy symbols must be transferred from the DDSP to the ERCO.

12.4.3. TRANSFER OF SETTINGS

Settings are sent to the ERCO via the serial data line SETDAT.



There are seven settings, divided into two groups:

– ERCO SETTINGS

DIST7: selects the Reed Solomon code, RS(32,28,5) or RS(32,26,7). DIST7 = "1" means RS(32,28,7) mode.
DEC: Selects code mode (recording) or decode mode (playback). DEC = "1" means playback.

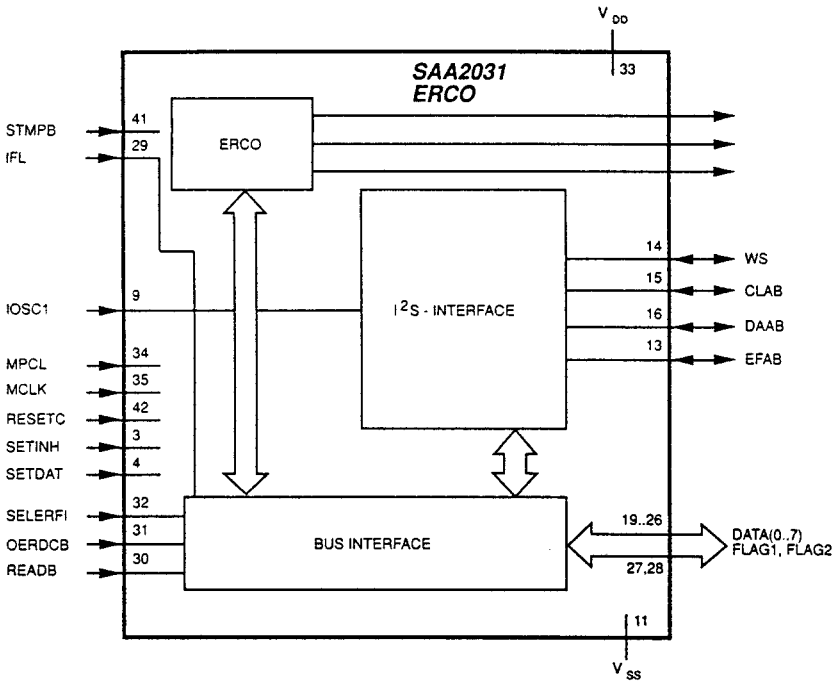
– I²S-INTERFACE SETTINGS

PLB: selects I²S-interface / FIFO data recording or playback mode. PLB = "1" sets the data flow direction from the data bus via the FIFO to the I²S-interface (i.e. for recording).
ANREC: specifies the master of the I²S-interface for recording. ANREC is normally "0", meaning slave mode.
WSFR0, WSFR1: define the word selection frequency of the I²S-interface. If WSFR0 = "0" and WSFR1 = "0", the word selection frequency is 48kHz. IOSC1 is the SBMCLK input signal of the SBC.
PERWORD: During playback, 16-bit words are transferred via the I²S-interface, and the associated error flags via EFAB. If PERWORD = "1", these error flags each relate to 16 bits, and if PERWORD = "0" they relate to 8 bits. As error correction in DCC is also done by byte, **PERWORD** is usually 0 here.
SETINH: is directly connected to the DDSP output pin INHERCO. If SETINH = "1", settings are transferred.
New ERCO settings are valid from the next STMPB pulse. New I²S-interface settings are valid from the next STMPB pulse, or a RESETC pulse.

12.4.4. ERCO CONTROL LINES

IFL: is directly connected to the DDSP. The IFL (imposed) flag indicates that the symbol being sent to the ERCO at this moment is a parity word.
STMPB: STMPB = "0" starts the calculation of a new code word, and activates new settings for both I²S-interfaces of the ERCO.
RESETC: This reset pin stops the momentary activities of the ERCO, sets the FIFO to half the filling level, and activates new I²S-settings.

12.4.5. BLOCK DIAGRAM AND PIN CONFIGURATION



1	TEST1	do not connect
2	TEST2	do not connect
3	SETINH	ERCO (SAA2031) setting transfer inhibit signal (CMOS input levels)
4	SETDAT	data settings to settings register (CMOS input levels)
5	TEST3	do not connect
6	TEST4	do not connect
7	TEST5	do not connect
8	TEST6	do not connect
9	IOSC1	crystal oscillator1 input
10	TEST7	do not connect
11	Vss	supply ground (0V)
12	TEST8	do not connect
13	EFAB	I²S-interface error flag output to interpolator
14	WS	I²S-interface word selection fs (3-state inputs and outputs; CMOS levels)
15	CLAB	I²S-bus bit clock (3-state inputs and outputs; CMOS levels)
16	DAAB	I²S-bus serial data (3-state inputs and outputs; CMOS levels)
17	TEST9	do not connect
18	TEST10	do not connect
19	DATA0	0-th bit of databus (3-state output and input; TTL input levels, CMOS output levels)
20	DATA1	1-st bit of databus (3-state output and input; TTL input levels, CMOS output levels)
21	DATA2	2-nd bit of databus (3-state output and input; TTL input levels, CMOS output levels)
22	DATA3	3-rd bit of databus (3-state output and input; TTL input levels, CMOS output levels)
23	DATA4	4-th bit of databus (3-state output and input; TTL input levels, CMOS output levels)
24	DATA5	5-th bit of databus (3-state output and input; TTL input levels, CMOS output levels)
25	DATA6	6-th bit of databus (3-state output and input; TTL input levels, CMOS output levels)
26	DATA7	7-th bit of databus (3-state output and input; TTL input levels, CMOS output levels)
27	FLAG1	data bus flag1 (3-state output and input; TTL input levels, CMOS output levels)
28	FLAG2	data bus flag2 (3-state output and input; TTL input levels, CMOS output levels)
29	IFL	imposed flag, parity position (CMOS input levels)
30	READB	read enable signal for ERCO (SAA2031) from data-bus (CMOS input levels)
31	OERDCB	output enable signal for ERCO (SAA2031) from data-bus (CMOS input levels)
32	SELERFI	select between ERCO and FIFO (high=ERCO) (CMOS input levels)

33	VDD	positive supply voltage (+5V)
34	MPCL	3,072MHz clock phase reference (CMOS input levels)
35	MCLK	6.144MHz master clock input (CMOS input levels)
36	NER0	number of erasure indicator bit 0 output
37	NER1	number of erasure indicator bit 1 output
37	NER2	number of erasure indicator bit 2 output
39	TEST11	do not connect
40	TEST12	do not connect
41	STMPB	start ERCO (SAA2031) processing program (CMOS input levels)
42	RESETC	reset ERCO (SAA2031), set FIFO to half-full (CMOS input levels)
43	TEST13	do not connect
44	TEST14	do not connect

12.5. SAA2041 – Digital drive signal processing

The DDSP has three different operating modes:

– DPAP - data playback, aux playback

In this mode, the regenerated data of the 9 data tracks are demodulated by the DDSP, and stored temporarily in the DRAM. Error correction is then carried out, during which the DDSP controls the data flow to and from the ERCO. After a tape frame has been decoded, the PASC data is transferred to the SBC via the I²S-interface of the ERCO. The DDSP sends AUX and sysinfo data to the microprocessor via the LT-interface.

– DPAR - data playback, aux record

In this mode, the microprocessor writes AUX data to the DDSP, and reads sysinfo data from it. The regenerated digital signals of the 8 main data tracks are demodulated, and stored temporarily in the DRAM. Error correction is carried out with the ERCO (controlled by the DDSP). The PASC data is then transferred to the SBC via the I²S-interface of the ERCO. Simultaneously, the AUX data is formatted into a tape block, adding block headers, ETM, sync pattern and IFG. The tape blocks are passed on to the write amplifier.

– DRAR - data record, aux record

In this mode, PASC data is written via the I²S-interface of the ERCO to the DDSP, and then into the DRAM. AUX and sysinfo data is received from the microprocessor via the LT-interface and also stored in the DRAM. Error coding is carried out by the ERCO (controlled by the DDSP). The DDSP then forms the data in the DRAM into a tape block, adding block headers, ETM, sync pattern and IFG. Once the originally serial data has been coded, it is sent to the write amplifier in time-multiplexed form.

– AUX transfers

A maximum of 4 x 36 bytes per tape frame is transferred to or from the microprocessor. A block of 36 bytes takes 42,7msec.
AUX recording: Immediately after the start of a new program segment (STRTSEG = "1" for 650nsec), the first AUX byte is sent to the DDSP. Subsequent bytes are transferred with an interval <75µsec between bytes.

– Sysinfo transfers

The length of a sysinfo tape frame is 128 bytes, and it is transferred in 4 blocks of 32 bytes.
Sysinfo recording: After the start of a new program segment (STRTSEG = "1" for 650nsec), the first sysinfo byte is sent to theDDSP. Subsequent bytes are transferred with an interval <75µsec between bytes.
Sysinfo playback: 108µsec after STRTSEG, the first byte is sent from the microprocessor to the DDSP. Subsequent bytes are transferred with an interval <75µsec between bytes.

12.5.1. DATA TRANSFER FROM DEQ2 TO DDSP

Data is transferred from the DEQ2 to the DDSP via the data lines TCH0..TCH7 (main data) and TAUX (AUX data).

12.5.2. DATA TRANSFER BETWEEN DDSP AND ERCO

Data is transferred between the DDSP and the ERCO via a 10-bit parallel bus, which consists of data lines ED0..ED9. The ERCO reads data from the bus if READB = "0", and writes it if OERDCB = "0". READB and OERDCB can never be "0" simultaneously!

The control line SELERFI gives the type of data. If SELERFI = "1", it is error correction data. If SELERFI = "0", data is written to or read from the I²S-interface of the ERCO.

The operating mode of the ERCO is determined by settings which the DDSP sends to the ERCO via SETERCO. Apart from code/decode mode, these settings also give the RS distance (5 or 7) and the data transfer direction of the I²S-interface. When settings are being sent, INHERCO = "1".

In ERCO code mode, the IFL line of the DDSP indicates that the data which has just been transferred is parity information.

The coding/decoding program of the ERCO is started each time the DDSP sets STMPB = "0".

RESETC from the DDSP causes the ERCO to be reset.

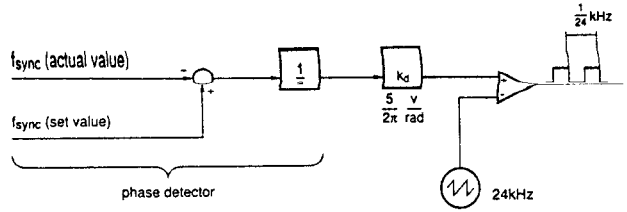
12.5.3. DATA TRANSFER BETWEEN DDSP AND DRAM

The DDSP uses a 64k x 4 bit dynamic RAM in page mode. Access time = 80..120 msec, refresh time = about 4msec. Data is transferred to and from the DRAM in bursts of 3 nibbles.

12.5.4. CAPSTAN MOTOR CONTROL

The SPEED signal is a pulse width modulated output signal for phase control of the capstan. A pulse dutyfactor of 50% corresponds to the nominal tape speed of 4,76 cm/sec. In search mode (tape speed 3..50 times faster), the tape does not touch the capstan shaft, so search mode is unregulated.
The extreme values of the pulse duty factor are 0% and 100%.
Pulse duty factor = 0% if the information comes from the tape too early → linear reduction of pulse duty factor.
Pulse duty factor = 100% means that the information comes from the tape 2 tape blocks too late.

Control loop:



1 tape block = 5,31msec
Frequency range at 48kHz = 20,83msec, i.e. frequency range of PLL 2 tape blocks.

If the tape speed deviates from the nominal value by more than 10%, the phase detector retains its last value. The phase detector (which is integrated in the IC) is unstable at certain frequencies, so a special control circuit is required.

12.5.5. DATA TRANSFER BETWEEN DDSP AND MICROPROCESSOR

Data is exchanged between the DDSP and the microprocessor via the bus lines LTCLK (clock), LTDATA (data) and LTEN (enable), and the control lines LTCNT0, LTCNT1 and STRTSEG.
LTCLK is provided by the microprocessor. The data bytes transferred via LTDATA are transmitted first with the LSB. LTEN indicates which IC is addressed via the LT bus.
LTCNT0 and LTCNT1 indicate the type of data transferred:

LTCNT1	LTCNT0	AUX	DATA	FROM	TO	TRANSFER OF
0	0	x	record	µP	DDSP	SYSINFO
0	0	x	play	DDSP	µP	SYSINFO
0	1	record	x	µP	DDSP	AUX
0	1	play	x	DDSP	µP	AUX
1	0	x	x	µP	DDSP	Settings
1	1	x	x	DDSP	µP	Status

The STRTSEG output of the DDSP is used as the time reference for the exchange of AUX and sysinfo data between the microprocessor and the DDSP. Every 42,7msec, this signal = "1" for 650nsec. STRTSEG is used as an interrupt for the microprocessor.

12.5.6. TRANSFER OF SETTINGS (LTCNT1 = "1", LTCNT0 = "0")

The setting bits determine the operating mode of the DDSP.

BIT	NAME	DESCRIPTION	DEFAULT
0	NOMSPD	Nominal tape speed	0
1	NOCOS	Disable error correction	0
2	ZFDA	Zero fill data in record	0
3	RECLAB	Record label	0
4	AUXPLB	AUX playback	1
5	DATAPLB	DATA playback	1
6	SETPIN1	Output port expander pin 1	0
7	SETPIN2	Output port expander pin 2	0

NOCOS - for testing purposes only.
ZFDA - for testing purposes only.
NOMSPD - NOMSPD = "1" sets the pulse duty factor of the speed control to 50% (used in recording mode)
RECLAB - during AUX recording, writes a label ID. If RECLAB = "1", a body is written for every AUX tape block. If RECLAB = "0", a body is written for AUX tape blocks 0 and 2 only.
AUXPLB - "1" = AUX playback, "0" = AUX recording.
DATAPLB - "1" = DATA playback, "0" = DATA recording.
SETPIN1 - port expander bit 1.
SETPIN2 - port expander bit 2.

The following table shows typical settings in the various operating modes:

BIT	7	6	5	4	3	2	1	0
Data and AUX playback	x	x	1	1	x	x	0	0
Data and AUX recording, no label	x	x	0	0	0	0	0	0
Data and AUX recording, label	x	x	0	0	1	0	0	0
Data playback and AUX recording, no label	x	x	1	0	0	0	0	1
Data playback and AUX recording, label	x	x	1	0	1	0	0	1

12.5.7. INTERROGATION OF STATUS INFORMATION (LTCNT1 = "1", LTCNT0 = "1")

The DDSP generates two different status words, which can be interrogated by the microprocessor.
Status word 0 has the following meanings:

BIT	NAME	DESCRIPTION
0	SEG0	Program segment number (LSB)
1	SEG1	Program segment number (MSB)
2	URDA	Data from DDSP (SAA2041) is unuseable
3	SEARLAB	Label flag during search
4	AUXFL0	AUX error flag 0
5	AUXFL1	AUX error flag 1
6	SYSFL	Instantaneious SYSINFO error flag
7	SYSFLC	cumulative SYSINFO error flag

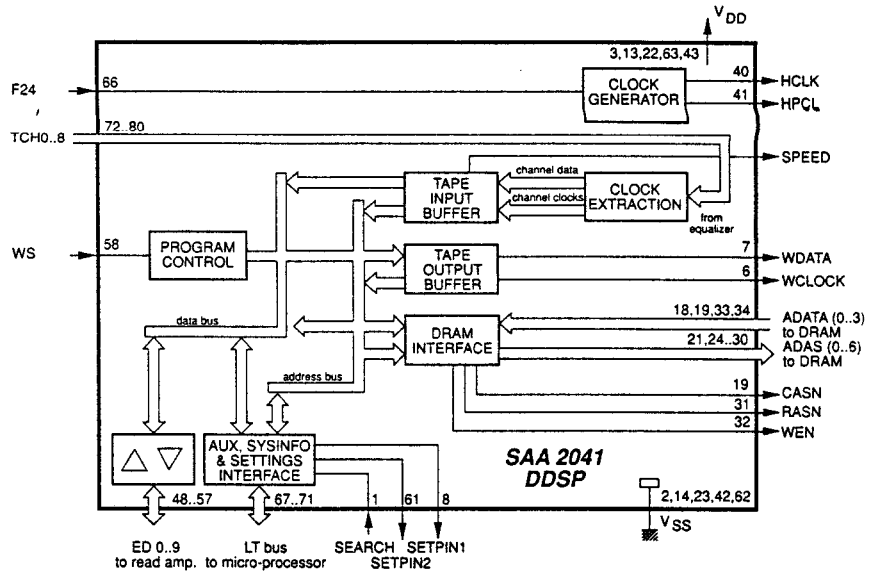
SEG0 and SEG1 identify one of the 4 program segments of the DDSP.
URDA is generated by PRGMAN, and signals that themain, sysinfo and AUX data are unuseable, independently of other flag information. URDA occurs at a change from recording to playback, or resynchronisation of the system.
AUXFL0 and AUXFL1 are only used during AUX playback, and signal that code words 0/1 of an AUX tape block to be transferred are faulty.
SYSFL and SYSFLC are only used during data playback. SYSFL signals an error in the next sysinfo byte to be transmitted. SYSFLC signals a faulty sysinfo byte in the transferred segment.
SEARLAB is read in search mode, and shows the status of SEARCHIN, the label detection at the tape position at that moment.

Status word 1 has the following meanings:

BIT	NAME	DESCRIPTION
0	STRGL0	Channel 0 C1 flag check
1	STRGL1	Channel 1 C1 flag check
2	STRGL2	Channel 2 C1 flag check
3	STRGL3	Channel 3 C1 flag check
4	STRGL4	Channel 4 C1 flag check
5	STRGL5	Channel 5 C1 flag check
6	STRGL6	Channel 6 C1 flag check
7	STRGL7	Channel 7 C1 flag check

The C1-error flag indicate errors in the channel data transmittet and are valid for each tape frame. The flags are only output during playback, and are a measure of the reliability of the data channels.

12.5.8. BLOCK DIAGRAM AND PIN CONFIGURATION



1	SEARCH	search label detection input (TTL-level)
2	Vss	supply ground (0V)
3	VDD	positive supply voltage (+5V)
4	TEST0	do not connect
5	TEST1	do not connect
6	WCLOCK	bit-clock for transfers to write amplifier (push-pull output)
7	WDATA	serial data to write amplifier (push-pull output)
8	SETPIN1	microprocessor expander pin (push-pull output)
9	SPEED	pulse width modulated output for tape speed control (push-pull output)
10	AZCHK	tape channels 0-7 azimuth monitoring (push-pull output)
11	PRGSTAT	DDSP program status (push-pull output)
12	TEST2	do not connect
13	VDD	positive supply voltage (+5V)
14	Vss	supply ground (0V)
15	TEST3	do not connect
16	TEST4	do not connect
17	TEST5	do not connect
18	RDATA3	data-bus connected to DRAM (3-state push-pull output and input; TTL-level)
19	CASN	column address strobe for DRAM (push-pull output)
20	RDATA2	data-bus connected to DRAM (3-state push-pull output and input; TTL-level)
21	ADRS0	DRAM address (push-pull output)
22	VDD	positive supply (+5V)
23	Vss	supply ground (0V)
24	ADRS1	DRAM address (push-pull output)
25	ADRS2	DRAM address (push-pull output)
26	ADRS3	DRAM address (push-pull output)
27	ADRS7	DRAM address (push-pull output)
28	ADRS4	DRAM address (push-pull output)
29	ADRS5	DRAM address (push-pull output)
30	ADRS6	DRAM address (push-pull output)
31	RASN	row address strobe for DRAM (push-pull output)
32	WEN	active low enabling for DRAM (push-pull output)
33	RDATA1	data bus connected to DRAM (3-state push-pull output and input; TTL-level)
34	RDATA0	data bus connected to DRAM (3-state push-pull output and input; TTL-level)
35	CEN	active low to enable DRAM (push-pull output)
36	SETERCO	ERCO (SAA2031) serial settings (push-pull output)
37	INHERCO	active low inhibit for transfer settings to ERCO (SAA2031) (push-pull output)
38	RESETC	ERCO (SAA2031) reset (push-pull output)
39	STMPB	start ERCO (SAA2031) program (push-pull output)

40	MCLK	clock output to ERCO (SAA2031) (push-pull output)
41	MPCL	ERCO (SAA2031) clock phase reference (push-pull output)
42	Vss	supply ground (0V)
43	VDD	positive supply (+5V)
44	SELERFI	ERCO (SAA2031) and I²S-FIFO transfers (push-pull output)
45	OERDCB	ERCO (SAA2031) active low enable (push-pull output)
46	READB	active low to enable ERCO (SAA2031) data bus to be read (push-pull output)
47	IFL	ERCO (SAA2031) imposed flag (push-pull output)
48	ED9	ERCO (SAA2031) data bus (3-state push-pull output and input; TTL-level)
49	ED8	ERCO (SAA2031) data bus (3-state push-pull output and input; TTL-level)
50	ED7	ERCO (SAA2031) data bus (3-state push-pull output and input; TTL-level)
51	ED6	ERCO (SAA2031) data bus (3-state push-pull output and input; TTL-level)
52	ED5	ERCO (SAA2031) data bus (3-state push-pull output and input; TTL-level)
53	ED4	ERCO (SAA2031) data bus (3-state push-pull output and input; TTL-level)
54	ED2	ERCO (SAA2031) data bus (3-state push-pull output and input; TTL-level)
55	ED3	ERCO (SAA2031) data bus (3-state push-pull output and input; TTL-level)
56	ED1	ERCO (SAA2031) data bus (3-state push-pull output and input; TTL-level)
57	ED0	ERCO (SAA2031) data bus (3-state push-pull output and input; TTL-level)
58	WS	I²S-interface word selection for DDSP (SAA2041) software program synchronization (CMOS input)
59	SBPLB	SBC (SAA2021) control signal indicating direction of data flow on I²S-interfaces between ERCO (SAA2031) and SBC (SAA2021) (push-pull output)
60	MUTE	"unreliable" data signal to SBC (SAA2021) (push-pull output)
61	SETPIN2	microprocessor port expander pin (push-pull output)
62	Vss	supply ground (0V)
63	VDD	positive supply (+5V)
64	STRTSEG	timing reference for microprocessor data transfers (push-pull output)
65	RESET	DDSP reset (CMOS input with pull-down and hysteresis)
66	f24	clock input (CMOS input)
67	LTDATA	LT-interface data line (3-state push-pull output and input; TTL-level)
68	LTCNT1	LT-interface control lines (TTL input)
69	LTCNT0	LT-interface control lines (TTL input)
70	LTCLK	LT-interface bit clock (TTL input)
71	LTEN	LT-interface device enable (TTL input)
72	TCH8	channel 0-7 input from equalizer (CMOS input)
73	TCH7	channel 0-7 input from equalizer (CMOS input)
74	TCH6	channel 0-7 input from equalizer (CMOS input)
75	TCH5	channel 0-7 input from equalizer (CMOS input)
76	TCH4	channel 0-7 input from equalizer (CMOS input)
77	TCH3	channel 0-7 input from equalizer (CMOS input)
78	TCH2	channel 0-7 input from equalizer (CMOS input)
79	TCH1	channel 0-7 input from equalizer (CMOS input)
80	TCH0	channel 0-7 input from equalizer (CMOS input)

12.6. SAA2051 - Digital equalizer

The DEQ2 has three different operating modes:

– Data playback

During playback, the following steps are carried out in the DEQ2:

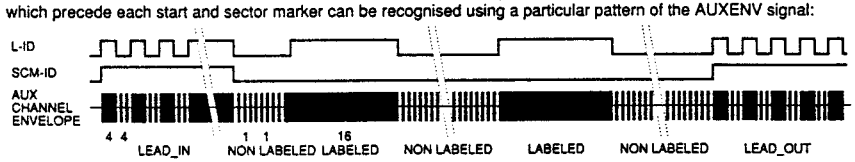
1. A/D conversion
   The RDMUX signal supplied by the read amplifier is first A/D converted in the DEQ2. The sampling frequency of the ADC is synchronous with the switching frequency of the multiplexer, and therefore synchronous with RDCLK (3,072MHz). For each cycle of RDSYNC, 10 slots are transferred (8 main data, AUX, dummy).
2. Demultiplexing
   The analogue head signals are transferred from the read amplifier to the DEQ2 in 10 slots (8 main data, AUX, dummy). The tape signals, which have meanwhile been A/D converted, are further processed in parallel by the following stages, so they must be demultiplexed.
3. Equalisation
   Two digital filters (IIR and FIR) provide optimum decision windows.
4. Zero crossing

– Search mode

In this mode, start and sector markers can be read from the tape (feature markers are recognised in playback mode only). It also recognises whether an unrecorded tape is being read, and outputs a corresponding control signal (VIRGIN). In search mode, the DEQ2 operates as follows:

1. A/D conversion
2. Demultiplexing
3. Envelope detection

After A/D conversion and isolation of the AUX channel, the envelope of the AUX data (AUXENV) is examined. The label IDs which precede each start and sector marker can be recognised using a particular pattern of the AUXENV signal:



However, since the search speed can be 3..50 times the nominal tape speed of 4,76 cm/sec, the current tape search speed must be evaluated in parallel. The tape speed at that moment is calculated from the signals from two light barriers in the drive.

– Off mode

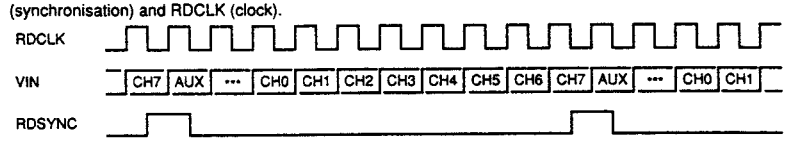
In this mode, RDSYNC and RDCLK = "1", the eye outputs are disabled, and the outputs CH0..CH7 and AUX are tristated.

12.6.1. DATA TRANSFER FROM DEQ2 TO DDSP

Data is transferred from the DEQ2 to the DDSP via the data lines TCH0..TCH7 (main data) and TAUX (AUX data).

12.6.2. DATA TRANSFER FROM READ AMPLIFIER TO DEQ2

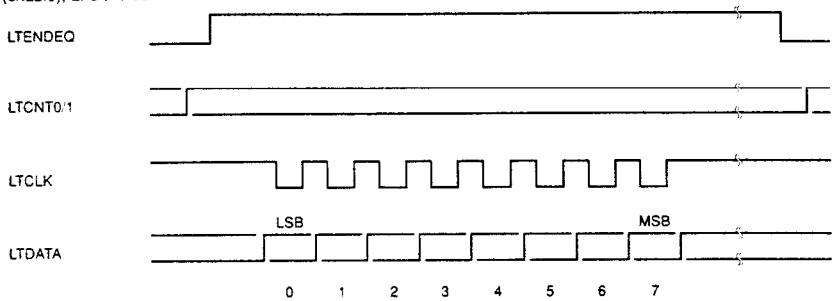
Data is transferred from the read amplifier to the DEQ2 via the data lines VIN (analogue, time-multiplxed head data), RDSYNC (synchronisation) and RDCLK (clock).



For every cycle of RDSYNC (307,2kHz), the information of 8 main data tracks, the AUX track and one dummy slot is transferred. When RDSYNC = "1", the head signals of the AUX channel are transferred. The data is read in at each rising edge of RDCLK.

12.6.3. DATA TRANSFER BETWEEN DEQ2 AND MICROPROCESSOR

Data is exchanged between the DEQ2 and the microprocessor via the bus lines LTCLK (clock), LTDATA (data) and LTENDEQ (enable), and the control lines LTCNT0 and LTCNT1.



LTCNT0 and LTCNT1 indicate the type of data transferred:

LTCNT1	LTCNT0	LT-DATA MODE	FROM	TO	TRANSFER OF
0	0	data write	µP	DEQ2	data
0	1	data read	DEQ2	µP	data
1	0	address write	µP	DEQ2	address
1	1	mode settings write	µP	DEQ2	mode settings

Before each data transfer, the master first sets the mode (control lines LTCNT0 and LTCNT1). LTENDEQ is set to "1", and the selected mode is activated by the positive edge. The master now provides the clock (LTCLK), and sends / receives the information to / from the slave. The data is always transferred in units of 8 bits, LSB first.

12.6.4. TRANSFER OF MODE SETTINGS (LTCNT1 = "1", LTCNT0 = "1")

8 bits are transferred to set both the operation modeand the data exchange type.

MSB LSB

x	x	x	x	b1	b0	a1	a0

Bits a0..a1 set the operating mode of the DEQ2, and have the following meanings:

a1	a0	OPERATION MODE
0	0	normal
1	0	search
1	1	off

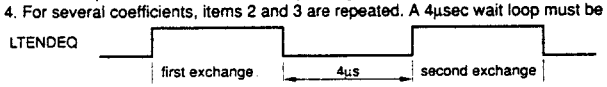
Bits b0..b1 give the type of settings transferred and the transfer direction:

b1	b0	DATA	EXCHANGE	TYPE
0	0	write	coefficient	data
0	1	read	coefficient	data (see note)
1	1	read	envelope	data

Note: after communication sequence the data exchange type must be set to "read coefficient data".

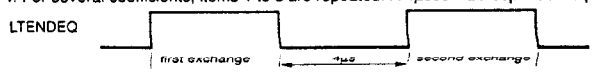
12.6.5. TRANSFER OF FILTER COEFFICIENTS

New filter coefficients are written from the microprocessor to the DEQ2 in the following sequence:
1. The microprocessor sends the mode settings to the DEQ2: b1 = "0", b0 = "0". (LTCNT1 = "1", LTCNT0 = "1")
2. The microprocessor sends the coefficient address to the DEQ2. (LTCNT1 = "1", LTCNT0 = "0")
3. The microprocessor sends the corresponding coefficient to the DEQ2. (LTCNT1 = "0", LTCNT0 = "0")
4. For several coefficients, items 2 and 3 are repeated. A 4µsec wait loop must be provided between two write cycles.



5. The microprocessor sends the mode settings to the DEQ2: b1 = "0", b0 = "1". (LTCNT1 = "1", LTCNT0 = "1")

The current filter coefficients of the DEQ2 can be read from the microprocessor in the following sequence:
1. The microprocessor sends the desired coefficient address to the DEQ2. (LTCNT1 = "1", LTCNT0 = "0")
2. The microprocessor sets LTCNT1 = "0", LTCNT0 = "1" (data read).
3. The DEQ2 sends the filter coefficient to the microprocessor. (LTCNT1 = "0", LTCNT0 = "1")
4. For several coefficients, items 1 to 3 are repeated. A 4µsec wait loop must be provided between two read cycles.



The coefficient address consists of two units of 4 bits, which are transferred as an 8-bit word:

MSB LSB

c3	c2	c1	c0	t3	t2	t1	t0

Bits c3..c0 are the channel number (0000..0111 for main data tracks, 1000 for the AUX track).
Bits t3..t0 are the so-called tap number (0000..1011).

The filter coefficients are integers between -128 and +127, and are transferred as 8-bit words:

MSB LSB

d7	d6	d5	d4	d3	d2	d1	d0

12.6.6. TRANSFER OF TAPE SPEED DATA (not used)

MSB LSB

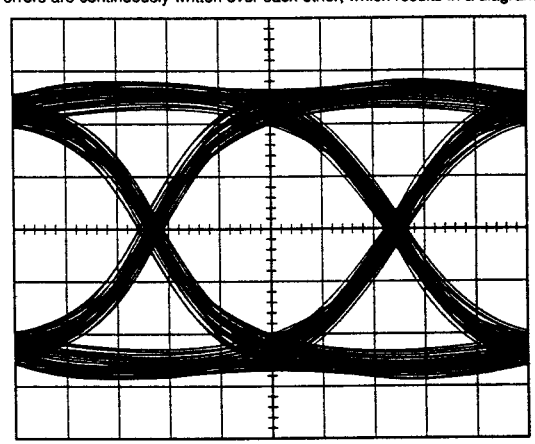
SVF	SC4	SC3	SC2	SC1	SC0	SR1	SR0

12.6.7. READING THE ENVELOPE DATA

Sequence:
1. The microprocessor sends the mode settings to the DEQ2 (b1 = "1", b0 = "1", LTCNT1 = "1", LTCNT0 = "1").
2. The DEQ2 sends the envelope data to the microprocessor (LTCNT1 = "0", LTCNT0 = "1").
3. The microprocessor sends the mode settings to the DEQ2 (b1 = "0", b0 = "1", LTCNT1 = "1", LTCNT0 = "1").

12.6.8. EYE OSCILLOGRAM

The analog head signals are distorted by level oscillations, jitter effects and the band pass properties of the transmission path. A method of judging the quality of the head signals is provided by the so-called "eye diagram". This signal is created by synchronising the played-back head signal with the recovered clock signal. On the oscilloscope, pulses with level and phase errors are continuously written over each other, which results in a diagram which looks like this:



Essentially, two points are decisive for judging the quality of transfer:
1. The width of the area in the zero crossings of the signal corresponds to the phase jitter of the signal. In the ideal case, the bits cross the zero line in one point.
2. The vertical opening of the "eye" indicates differences of level between individual bits. In the ideal case, all bits have the same (maximum) signal amplitude.

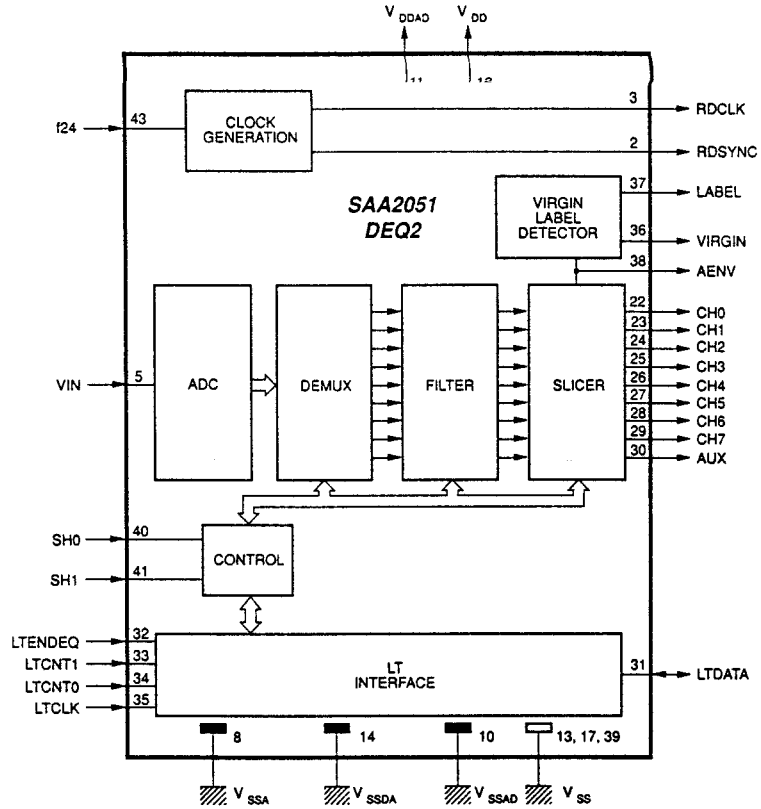
12.6.9. FILTER OUTPUT SCALING

The internal digital filters of the DEQ2 have a precision of 11 bits, but only an 8-bit "window" is used in further processing. The position of this window can be set externally by the control lines SH0 and SH1:

SH1	SH0	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0	*0*				x	x	x	x	x	x	x	x
0	1			x	x	x	x	x	x	x	x	
1	0		x	x	x	x	x	x	x	x		
1	1	x	x	x	x	x	x	x	x			

x indicates bit selected

12.6.10. BLOCK DIAGRAM AND PIN CONFIGURATION



1	TEST1	do not connect
2	RDSYNC	SYNC data for read amplifier (push-pull output)
3	RDCLK	data clock for read amplifier (push-pull output)
4	TEST2	connect to Vss
5	VIN	analog time multiplexed input from read amplifier
6	REFN	lower reference voltage (+1,5V) for ADC
7	REFP	upper reference voltage (+3,5V) for ADC
8	VssA	supply ground (0V)
9	BIASA	bias current for A/D-converter (sinks current from VDD via 12kΩ)
10	VssAD	supply ground (0V) for ADC
11	VDDAD	positive supply (+5V) for ADC
12	VDD	positive supply (+5V)
13	Vss	supply ground (0V)
14	VssDA	supply ground (0V) for DAC
15	TEST3	do not connect
16	BIASD	bias current (sources current to Vss via 2,75kΩ)
17	Vss	supply ground (0V)
18	TEST4	do not connect
19	TEST5	do not connect
20	TEST6	do not connect
21	TEST7	do not connect
22	CH0	channel 0 output for DDSP (SAA2041) (push-pull output)
23	CH1	channel 1 output for DDSP (SAA2041) (push-pull output)
24	CH2	channel 2 output for DDSP (SAA2041) (push-pull output)
25	CH3	channel 3 output for DDSP (SAA2041) (push-pull output)
26	CH4	channel 4 output for DDSP (SAA2041) (push-pull output)

27	CH5	channel 5 output for DDSP (SAA2041) (push-pull output)
28	CH6	channel 6 output for DDSP (SAA2041) (push-pull output)
29	CH7	channel 7 output for DDSP (SAA2041) (push-pull output)
30	AUX	AUX-channel output for DDSP (SAA2041) (push-pull output)
31	LTDATA	microcontroller I/O data interface (3-state push-pull output and input; CMOS levels)
32	LTENDEQ	microcontroller interface enabling (CMOS input levels)
33	LTCNT1	microcontroller interface; mode control 1 (CMOS input levels)
34	LTCNT0	microcontroller interface; mode control 0 (CMOS input levels)
35	LTCLK	microcontroller bit-clock interface (CMOS input levels)
36	VIRGIN	search mode virgin detection output
37	LABEL	search mode label detection output
38	AENV	search mode auxiliary detection output
39	Vss	supply ground (0V)
40	SH0	shift0, equalized channel resolution input
41	SH1	shift1, equalized channel resolution input
42	TEST8	test input to be connected to Vss
43	f24	clock input; typical frequency 24,576 MHz (CMOS input)
44	TEST9	do not connect

12.7. TDA1317 - Read amplifier

Tasks of the read amplifier:
The head signals of the digital magneto-resistive heads (MRH) have only small AC amplitudes (in tens of microvolts). The read amplifier is responsible for the amplification and filtering of the MRH head signals. The following components are implemented in the IC:

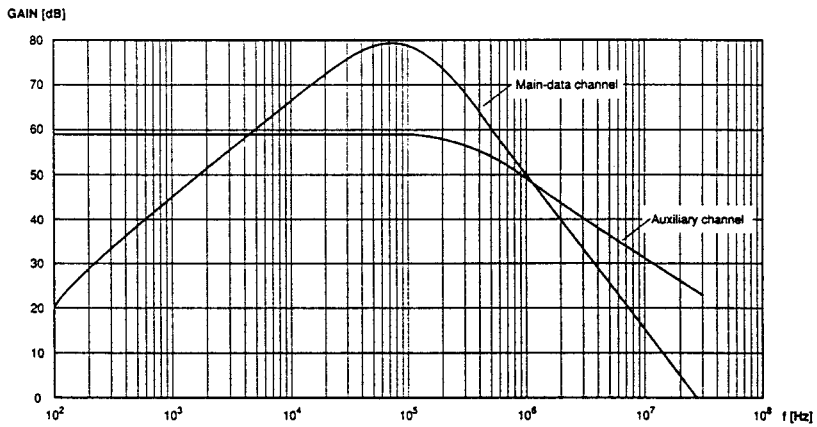
12.7.1. PRE-AMPLIFIERS FOR 8 DIGITAL MRHs OF MAIN DATA TRACKS

The head signals are first amplified by 58dB by low noise pre-amplifiers, downstream of which a low pass filter stage with a limit frequency of 135kHz and a high pass filter stage with a limit frequency of 80kHz are connected. This is followed by a further amplification by 26dB, and a second 135kHz low pass filter. The two low pass filters are for anti-aliasing, and the high pass filter is for pre-equalizing of the head signals.

12.7.2. PRE-AMPLIFIER FOR MRH OF AUX CHANNEL

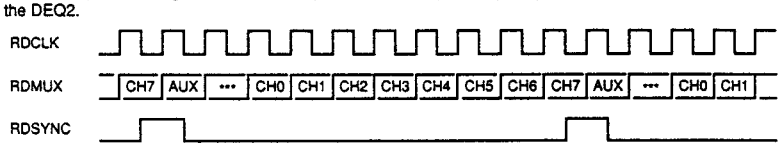
The head signal of the AUX track is first amplified by 58dB, and filtered by a 400kHz low pass filter.

Frequency response of amplifier and filter stages for main data and AUX channels:



12.7.3. MULTIPLEXER

The amplified and filtered analogue head signals ofthe nine digital tracks are transferred in serial form to the DEQ2 via RDMUX. For this purpose, the signals must be multiplexed. The multiplex frequency is 3,072MHz, and is synchronous with the RDCLK of the DEQ2.



For every cycle of RDSYNC (307,2kHz), the information of 8 main data tracks, the AUX track and one dummy slot is transferred. When RDSYNC = "1", the head signals of the AUX channel are transferred. The data is read in at each rising edge of RDCLK.

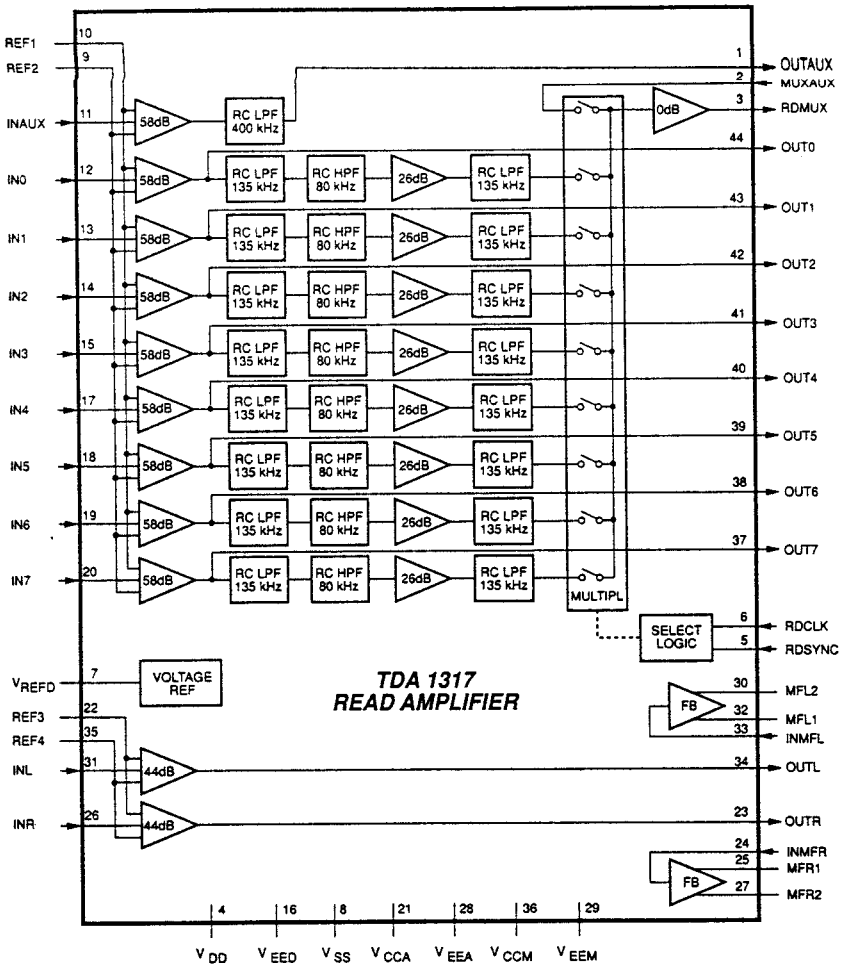
12.7.4. PRE-AMPLIFIERS FOR MRHS OF ANALOGUE TRACKS

Two low noise amplifier stages, which raise the AC signals by 44dB, are responsible for the pre-amplification of the head signals of the two analogue tracks.

12.7.5. FEEDBACK AMPLIFIERS

To linearise the frequency response of the analogue track MRHs, two so-called feedback amplifiers, which make possible a kind of magnetic feedback, are provided.

12.7.6. BLOCK DIAGRAM AND PIN CONFIGURATION



1	OUTAUX	auxiliary data output
2	MUXAUX	auxiliary multiplexer input
3	RDMUX	read multiplexer output
4	VDD	positive supply voltage DCC-part (+5V)
5	RDSYNC	read sync input
6	RDCLK	read clock input
7	VREFD	voltage reference (digital)
8	Vss	supply ground (0V)
9	REF2	reference voltage 2
10	REF1	reference voltage 1
11	INAUX	auxiliary data input
12	IN0	main data input 0
13	IN1	main data input 1
14	IN2	main data input 2
15	IN3	main data input 3
16	VEED	digital ground
17	IN4	main data input 4
18	IN5	main data input 5
19	IN6	main data input 6
20	IN7	main data input 7
21	VCCA	positive supply voltage CC-part (+5V)
22	REF3	reference voltage 3
23	OUTR	analog (CC) output right
24	INMFR	feedback amplifier input right
25	MFR1	feedback amplifier output right 1
26	INR	analog (CC) input right
27	MFR2	feedback amplifier output right 2
28	VEEA	analog ground
29	VEEM	ground for feedback amplifier
30	MFL2	feedback amplifier output left 2
31	INL	analog (CC) input left
32	MFL1	feedback amplifier output left 1
33	INMFL	feedback amplifier input left
34	OUTL	analog (CC) output left
35	REF4	reference voltage 4
36	VCCM	positive supply voltage feedback amplifier (+5V)
37	OUT7	main data output 7
38	OUT6	main data output 6
39	OUT5	main data output 5
40	OUT4	main data output 4
41	OUT3	main data output 3
42	OUT2	main data output 2
43	OUT1	main data output 1
44	OUT0	main data output 0

12.8. TDA1316T - Write amplifier

Tasks of the write amplifier:
The write amplifier is responsible for preparing the data of the nine digital write heads. The following circuit blocks are implemented in the IC:

12.8.1. CURRENT SOURCE

The value of the write current depends on the efficiency of the write heads and can be set to the required value by external circuitry. Values between 120 and 180mA are possible.

12.8.2. CLAMPING CIRCUIT

This internal circuit of the write amplifier switches an external resistive load to the current source, at times when no current is flowing through the write heads. In this way, there is a constant load on the source, which effectively suppresses interference.

12.8.3. SHORT-CIRCUIT PROTECTION

All write outputs of the write amplifier are short-circuit protected. If a fault occurs, the IC automatically switches off (V_0<1,2V).

12.8.4. DECODER

The write amplifier is controlled by a 32-bit word, which is sent serially by the DDSP via WDATA (clock frequency 3,072MHz). The write pulses are output at outputs QA..QJ. For timing, see 12.8.5.
As well as the digital head data, this signal also contains control bits, which set the mode of the write amplifier. Control bits TDAPLB, TAUPLB and TERAUX have the following meanings:

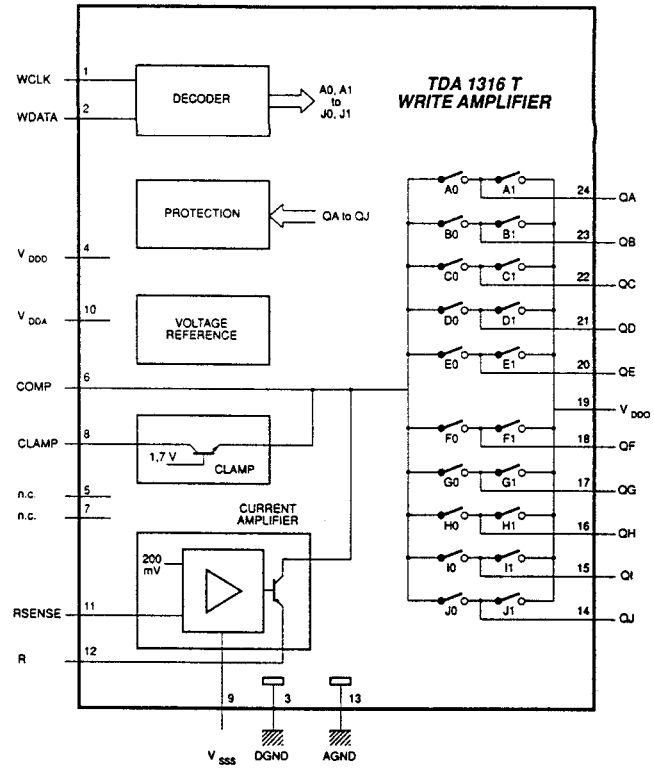
TDAPLB	TAUPLB	TERAUX	CHANNELS 0..7	AUX-CHANNEL
1	1	x	read	read
0	1	x	write	read
0	0	0	write	write
0	0	1	write	erase
1	0	0	read	write
1	0	1	read	erase

In standby mode (TDAPB = "1", TAUPLB = "1"), the internal current source of the IC is switched off.

12.8.5. TIMING

The individual channels are not addressed in parallel, but offset by 600nsec. This avoids unacceptable heating of the head. Depending on the data word, the tape is magnetized in the direction of movement or the reverse. If parts are to be erased (AUX erase), they are magnetized alternately with sequences of "0" and "1". The delete frequency is therefore 96 kbit/sec. The write time per bit is about 300nsec, and the gap between two successive bits on the tape is 10,41µsec at maximum (about 500nm). The short write time is sufficient, because the magnetization of the tape extends further in the direction of movement.

12.8.6. BLOCK DIAGRAM AND PIN CONFIGURATION



1	WCLK	write clock input
2	WDATA	write data input
3	DGND	digital ground
4	VDDD	positive supply voltage digital (+5V)
5	n.c.	not connected
6	COMP	frequency compensation
7	n.c.	not connected
8	CLAMP	voltage clamp
9	Vsss	sense voltage (ground)
10	VDDA	positive supply voltage analog (+5V)
11	RSENSE	feedback voltage
12	R	sense resistor
13	AGND	analog ground
14	QJ	write pulse output
15	QI	write pulse output
16	QH	write pulse output
17	QG	write pulse output
18	QF	write pulse output
19	VDDO	positive supply voltage write outputs
20	QE	write pulse output
21	QD	write pulse output
22	QC	write pulse output
23	QB	write pulse output
24	QA	write pulse output

12.9. M51581P - DIGITAL AUDIO INTERFACE (DAI)

Tasks of the DAI during recording:
In recording mode, the DAI demodulates the EBU-signal of the digital input and transfers the information to the SBF (audio data) resp. µP (U-bit and C-bit data). At the same time the system clock is reconstructed and the clock frequencies SCK/BCK and WS/LRCK are derived from this system clock. In case of recordings from an analog source, the A/D-converted analog signal is modulated according to the EBU-standard, first. Digital input signals can directly be copied to the digital output.

Tasks of the DAI during playback:
In playback mode, the DAI is exclusively responsible for modulation of the digital output data. The audio information sent by the SBF and the C-bit and U-bit data from the µP are input for the frame composition circuit of the DAI. The generated EBU-signal is then transferred to the digital output.

12.9.1. MODE SELECTION

In general, the DAI has four different operating modes, which can be selected via the mode selection pins MODE0 and MODE1:

MODE0	MODE1	MODE
0	0	µP-mode
0	1	easy mode
1	0	full transparent mode
1	1	test mode

In DCC devices, the DAI is operated in microprocessor mode, so the data transfers described in the following sections all assume this operating mode.

12.9.2. LT-INTERFACE

The control lines LTCNT0 and LTCNT1 indicate the type of data to be transferred via LTDATA to or from the microprocessor:

LTCNT1	LTCNT0	MODE	FROM	TO	TRANSFER OF
0	0	C-bit data	for further information see 9. Digital out		
0	1	U-bit data			
1	0	Settings	µP	DAI	8bits
1	1	Status	DAI	µP	8bits

12.9.3. TRANSFER OF SETTINGS (LTCNT1 = "1", LTCNT0 = "0")

This data consists of 8 information bits from the microprocessor to the DAI. These 8 bits have the following meanings:

BIT	NAME	DESCRIPTION
S0	TRAN/RECEP	Transmission/reception selection
S1	ADSEL	Polarity depends on ADSEL pin
S2	TEST	Only used for test purposses
S3	BCKPOL	Polarity of BCK select: "0"-falling edge at LRCK edge
S4	MUTE	Polarity depends on MUTE pin
S5	RXSEL	RX input selection, polarity depends on RXSEL pin
S6	TXOE	TX output enable
S7	OWD	Delay on information unit send action: "0"-no delay, "1"-4WS

12.9.4. INTEROGATION OF STATUS INFORMATION (LTCNT1 = "1", LTCNT0 = "1")

The DAI generates an 8-bit status word, which is continuously updated, and can be interrogated at any time by the µP.
These 8 bits have the following meanings:

BIT	NAME	DESCRIPTION
0	PLL UNLOCK	"0"-locked, "1"-not locked
1	FCHECK	Frequency check result: "0"-OK, "1"-error
2	DETFS0	Detected fs information bit0
3	DETFS1	Detected fs information bit1
4..7	-	Not used

DETFS0 and DETFS1 are coded as follows:

DETFS0	DETFS1	SAMPLING FREQU.
0	0	44,1kHz
0	1	not used
1	0	48kHz
1	1	32kHz

12.9.5. AUDIO INTERFACE "DIGITAL IN", "DIGITAL OUT"

The DAI is equipped with a digital interface, which allows data transfers between DAI and external sets with digital input and/or digital output. The data format is according to the EBU-standard (see also 9. Digital out).
Two digital inputs and one digital output are available:
- RX1 : Coaxial input (input level > 200mVpp)
- RX2 : Optical input (CMOS-input levels)
- TX : Digital output according to EBU-standard

The control line RXSEL sets the digital input (RXSEL = "1" for RX1, RXSEL = "0" for RX2).

12.9.6. RECONSTRUCTING OF THE SYSTEM CLOCK FROM AN EXTERNAL DIGITAL SOURCE

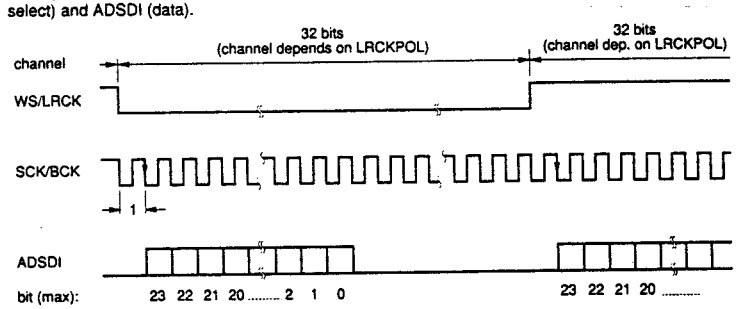
During recordings from an external digital source the system clock (256fs) has to be reconstructed from the EBU-signal. This is realized by a PLL-circuit. The phase detector of the PLL is already integrated in the DAI, the VCO has to be built-up external. The VCO frequency depends on the sampling frequency of the source. The highest VCO frequency is given at fs = 48kHz and will be 12,288MHz (thats 4 times the data rate of the EBU-signal).
In recording mode the clock signals SCK/BCK (64fs) and WS/LRCK (fs) are derived from the VCO frequency, in playback mode they are generated by the SBC.
If the PLL is locked the control line UNLOCK will be "0". At two successive recordings of different sampling frequency (e.g. 32kHz → 48kHz) the PLL needs a short time for resynchronization (about 50..100ms), UNLOCK will change to "1". Such short "unlocks" **must not** interrupt the recording, and are therefore ignored by the software.

12.9.7. CONTROL LINES OF THE AUDIO-INTERFACE

The audio data bus SCK/BCK (clock), WS/LRCK (word select) und SD/SDI resp. ADSDI (data) can be adapted to various applications by the following control lines:
- IIS : Selection of audio data format (IIS = "1" for I²S-format, IIS = "0" for non-I²S-format)
- ASL : Selection of audio sample length (ASL = "1" for 24bits, ASL = "0" for 16bits)
- LRCKPOL : Selection of word select polarity (LRCKPOL = "1" means at LRCK = "1" data of the left channel, LRCKPOL = "0" means at LRCK = "1" data of the right channel)
- MSBF : MSBF = "1" for MSB first, MSBF = "0" for LSB first
- CKSEL : Selection of master clock frequency (CKSEL = "1" for MSTCK = 128fs, CKSEL = "0" for MSTCK = 256fs)

12.9.8. TRANSMISSION OF AUDIO-BROADBAND SAMPLES FROM ADC TO DAI

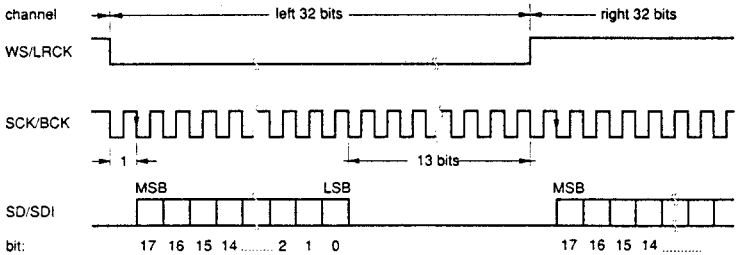
Analog input signals are digitized by the ADC. The samples are transmitted via the databus SCK/BCK (clock), WS/LRCK (word select) and ADSDI (data).



As already described in 12.9.7., the format of the audio data bus can be adapted. In DCC-sets these controls depend on the used SBFs, which require following mode: IIS = "1", ASL = "1", LRCKPOL = "0", MSBF = "1".

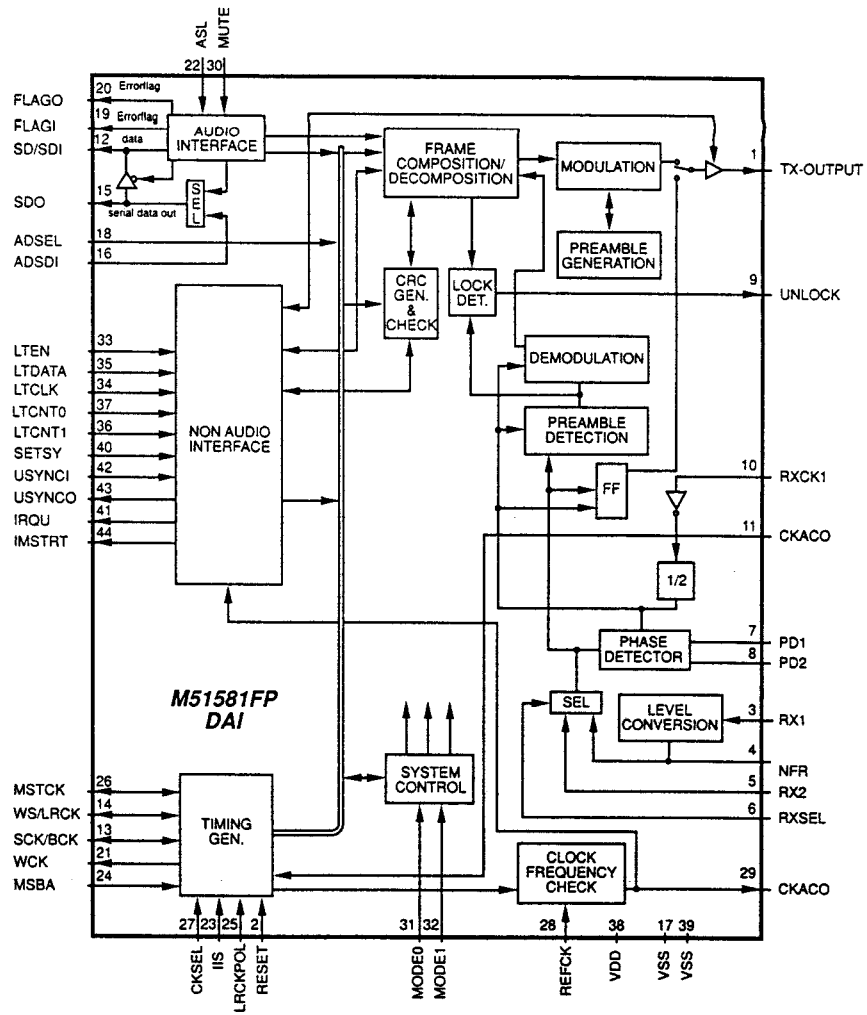
12.9.9. TRANSMISSION OF AUDIO BROADBAND SAMPLES TO AND FROM SBF

The audio broadband samples are input or output via the databus SCK/BCK (clock), WS/LRCK (word select) und SD/SDI (data) ("bi-directional").



The WS/LRCK signal is "0" when data of the left channel is transmitted, and "1" for the right channel. Its frequency is the sampling frequency fs. The clock frequency SCK/BCK is 64-times the sampling frequency.

12.9.x. BLOCK DIAGRAM AND PIN CONFIGURATION



1	TX	IEC format digital audio data output
2	RESET	DAI reset (µP mode: trans. mode, fs = 48kHz, TX not enabled)
3	RX1	IEC format digital audio data input1 for coaxial input (>200mVpp)
4	NFR	output of level converter for RX1
5	RX2	IEC format digital audio data input2 for optical input (CMOS logical level)
6	RXSEL	selection of RX1 or RX2 ("1" = RX1, "0" = RX2)
7	PD1	phase detector input for charge pump VCO
8	PD2	phase detector input for charge pump VCO
9	UNLOCK	indicates VCO frequency locked to RX data ("1" = not locked)
10	RXCKI	input of VCO frequency (256 x fs)
11	RXCKO	output of VCO frequency
12	SD/SDI	serial data input for audio data bus
13	SCK/BCK	shift/bit clock for audio data
14	WS/LRCK	word select for audio data ("0" = left channel)
15	SDO	serial data output for audio data bus

16	ADSDI	serial data input of AD-converter data
17	Vss	negative supply voltage
18	ADSEL	serial data output source selection ("1" = analog, "0" = digital)
19	FLAGI	error flag input
20	FLAGO	error flag output
21	WCK	word clock output (recp. mode only, 2 x fs)
22	ASL	audio sample length ("1" = 24bits, "0" = 16bits)
23	IIS	I²S-format selection ("1" = I²S, "0" = non-I²S)
24	MSBF	most significant bit first selection ("1" = MSBF, "0" = LSBF)
25	LRCKPOL	polarity of LRCK selection
26	MSTCK	master clock (128 or 256 x fs, according to CKSEL)
27	CKSEL	master clock frequency selection ("0" = 256 x fs, "1" = 128 x fs)
28	REFCK	reference clock for frequency accuracy check (norm. 9,408MHz)
29	CKACO	frequency accuracy check output ("1" = frequency deviation >0,14% - error condition)
30	MUTE	mute control ("1" = mute, "0" = no mute / mode00: mute polarity control)
31	MODE0	mode selection input0
32	MODE1	mode selection input1
33	LTEN	interface enable ("1" = enable)
34	LTCLK	interface data bit clock
35	LTDATA	interface data bus
36	LTCNT1	interface control1
37	LTCNT0	interface control0
38	VDD	positive supply voltage
39	Vss	supply ground (0V)
40	SETSY	settings sync. signal, latches new settings in internal register
41	IRQU	indicates information message can be read by µP (recp. mode) indicates information message sent (trans. mode)
42	USYNCI	indicates start of new frame (trans. mode)
43	USYNCO	indicates start of new frame (pecp. mode)
44	IMSTRT	start of new message on U bit indication

13. CIRCUIT DESCRIPTION 70DCC300/70DCC380

13.1. SUPPLY VOLTAGES

To supply the unit, the following **stabilized voltages** are produced at the **Main Board**:

+µP : Supply voltage for the 7335 (Main) and 7401 (Front) Microprocessors, for the Easy Link Interface and for the IR Eye. This voltage is available as soon as the mains switch is ON – also in the Standby mode.

+5V, -5V : Positive and negative supply voltage for the DOLBY IC on the Main Board and ICs on Read/Write and Digital Board.

+7V, -7V : Positive and negative supply voltage for the recording amplifier – analog input IC7302.

The voltages are derived from +12V and -12V. Both operational amplifiers of the IC7320 have been connected as voltage followers. The output voltage is determined by the voltage dividers R3171/R3173 and R3172/R3174. On the one hand, the voltage of ±7V guarantees maximum control of the A/D converter ($3,68V_{pp}$) whilst on the other preventing an input overload (max. $5,3V_{pp}$).

+12V, -12V : Positive and negative supply voltage for the operational amplifier, drive assembly and stabilization circuits on the Read/Write Board.

In order to suppress faults, the **Read/Write Board** is also provided with additional stabilization stages. All voltages are derived from the positive supply voltage **+12V**.
+12V → filtering → +10V → fixed voltage control for: **+5VA, +5VB, +7V**

The supply voltages for the Fluorescence Tube Display ("FTD") are fed via the Main Board (plug 1201/1252) to the Front Board (plug 1326/1425):

-30V : Cathode voltage for Display. Stabilization takes place at the Supply Board.
F1, F2 : Heating voltage for Display. There is an AC voltage of approx. 4V between F1 and F2.

Switching on the unit

Switching principle
The stabilized supply voltages are started up in the following sequence:
+µP, +5V switched by the Front Microprocessor 7401, **+12V, +7V** and the negative voltages **-12V, -5V** and **-7V** as a function of +5V.

If the mains switch is used to switch the unit on, the non-stabilized voltage **+5A** increases. The fixed voltage control 7201 is a low dropout type. For this reason the **+µP** voltage will follow with a mere -0,2V difference.
At the same time the muting, from which the Hardware Reset (HRESET) is derived, becomes active → see description for Mute circuits.
As soon as the supply for microprocessors, **+µP**, is stable, the Front Microprocessor 7401 is switched on via the HRESET connection and this sets the Standby-control output Pin 30 to LOW.
The basic current is now able to pass from T7202 via plugs 1425/1326 and R3202. Thus T7202 conducts and switches the stabilized voltage **+µP** to the emitter of T7200. Base current also passes via R3207 whilst T7200 also becomes conductive. Consequently T7204 and the series transistor 7203 in turn become conductive.
The emitter of T7200 is connected to the stabilized **+µP** voltage via the switching transistor 7202. The base of T7200 is "clamped" via diode 6209 to the collector of the series transistor 7203. Hence, if the output voltage at the collector of T7203 increases, the base voltage of T7200 will increase to the same extent. The base-emitter voltage of T7200 becomes weaker and T7200 conducts less. Consequently, both T7204 and the series transistor 7203 will conduct less.
The control loop for the **+5V** voltage is closed.
Because the supply to the emitter of T7200 is effected by **+µP**, the same approximate output voltage for **+5V** will be automatically set. The control accuracy is determined by the fixed voltage control 7201.
D6209 serves as temperature compensator for the BE section of T7200.
D6208 only operates in the event of a fault.
If the **+5V** voltage breaks down through being overloaded, fuses 1206 and 1207 will not interrupt if the unit is only operating on undervoltage. D6208 becomes conductive because of the low output voltage of **+5V**. Current now passes via T7202, T7200 and D6208 as well as from the fixed voltage control 7201 to the **+5V** load. The fixed voltage control 7201 is thus overloaded so that the integrated temperature controller regulates the output current – "fold back" characteristic.

As soon as the **+5V** voltage increases, current will pass through T7207 and R3213/R3214. This will cause T7207 to conduct. In turn, T7206 and the series transistor 7205 will become conductive. The **+12V** supply voltage will also start up, as a function of **+5V**. The output voltage of T7205 is determined by the voltage dividers R3212-R3213/R3214. Serving as reference is the supplyvoltage of the emitter of T7207 – i.e. **+5V**, which in turn (as described above) has **+µP** as its reference. The control accuracy of **+12V** is therefore also determined by the fixed voltage control 7201.

+7V and **-7V** increase owing to the voltage follower circuit with **+12V** and **-12V** (see below).
Although the positive supply voltages are relatively simple to start up in mutual dependence, this can only be ensured for the negative supply voltages by incorporating an extra switching transistor 7211.
Initially, the base of T7211 is negatively biased through R3215 to the unregulated **-12A** voltage and is therefore conductive. This causes the base of T7209 to be earthed – T7209 blocks and the control loop is not yet able to function.
Only once the positive supply voltage **+5V** builds up, will the voltage at the base of T7211 become positive through the voltage dividers D6208-R3208/R2115, and T7211 will block.
In the meantime the reference voltage at the emitter of the control transistor 7210 will have built up via the zener diode 6207, R3200 and R3219. Base current passes through the resistors R3222 and R3223, so that T7210 becomes conductive. As T7211 now blocks, T7209 and the series transistor 7208 will in turn be conductive.
The control loop is closed through the voltage dividers R3221-R3222/R3223.
An output voltage of **-12V** is set.
The fixed voltage control 7212 now also obtains its input voltage, so that the negative supply voltage **-5V** is able to start at the same time.

The circuit has been designed so that the positive and negative supply voltages are able to start up more or less at the same time and at the same speed. This guarantees that all the ICs are always connected to the same symmetrical supply.

13.2. MUTE CIRCUITS AND HARDWARE RESET

Two mute circuits with different tasks are to be found on the Main Board.

1) Muting for analog equalization

In order to prevent faults affecting SILENCE DETECTION (pause recognition), the ANALOG EQUALIZATION circuit will be muted as soon as a Digital Compact Cassette is used.

If a DCC is detected by the sensor in the drive, microprocessor 7335 will apply a LOW level at pin 6. This will cause T7315 to conduct and to switch through **+5V**. In consequence, T7311 and T7312 will also conduct and will mute the input of the analog-playback equalization amplifier.

2) Muting of the outputs FIX OUT, HEADPHONE and DIGITAL OUT

Muting prevents clicks during ON/OFF switching from reaching the output sockets. The control signal HRESET (Hardware Reset) is also obtained, which resets the Front Microprocessor and thus switches it on.

a) Switching the unit on with the mains switch (power on)

Please note that the following takes place in a very short time interval of less than 1 second.
After switching on the mains switch, the unregulated voltage **+5A** increases. The regulated **+µP** voltage derived from **+5A** follows with a difference of only 0,2V, because voltage control 7201 is a "low dropout" type. **+µP** reaches the emitter of T7349 via D6305 and the bases of T7350 and T7352 via R3250, R3387 and R3392. Both transistors start to conduct. Base current is able to pass from T7349 via R3259 and T7350. T7349 is now conductive and connects through all the MUTE transistors from T7341 up to T7348. The level at the collector of T7349 is now supplied as control signal DIGOFF to the Digital Board via plug 1323/1503 and transistors T7424, T7425 (protective function against negative voltages) also to the DAI (Pin 30).
The outputs FIX OUT, HEADPHONE and DIG OUT are muted.
By muting the analog outputs by 2 transistors each, a greater muting depth is obtained, which has been adapted to the dynamics of the unit.
When the **+5A** voltage reached approx. 5,2V, current passes through the zener diode 6307 (5V1 rated voltage).
Thus T7351 receives base current and switches through. T7350 and T7352 therefore block. T7349 remains conductive because C2294 is now charged by its base current.
Because T7352 is now blocking, C2389 is charged via R3249. The level on the HRESET line becomes HIGH, reaches Reset pin 12 of Front Microprocessor 7401 via plugs 1326/1425 and switches this on (LOW = Reset = switched off). After termination of the standard inquiries (cassette,...) the Front Microprocessor sends a reset pulse to the Main Microprocessor 7335 via the SRESET connection (software reset). The base of T7349 via R3260 is kept to LOW via the MUTE control output pin 21. The charging time of C2294 is just sufficient to bridge the time required for triggering the Main Microprocessors. Only after pressing the PLAY button and the start up of the drive will the Main Microprocessor connect the MUTE control output pin 21 to HIGH. T7349 therefore blocks. The bases of T7341 up to T7348 are all negatively biased via R3261. This will cause all transistors to block.
The Mute circuit is no longer active.

b) Switching the unit off with the mains switch (power off)

If the **+5A** voltage drops below approx. 5,2V after switching off, the current via zener diode 6307 will be too weak to allow T7351 to conduct any further. T7351 will block. The **+µP** voltage is still stable at this point. Transistors T7350 and T7352 are connected through via R3250, R3387 and R3392. Base current from T7349 passes via R3259 and T7350. T7349 connects through and hence so do T7341 up to T7348. The analog outputs and the digital output are muted.
As soon as T7352 is connected through, the HRESET line is LOW.
The Front Microprocessor recognizes via pin 1 (HRESET) that the unit has been switched off and sends a command to Microprocessor 7335 on the Main Board that the drive should be switched to STOP. Thus the Main Microprocessor 7335 is switched off via the SRESET connection.
With a time delay brought about by the RC section R3419/C2438, RESET input pin 12 of Front Microprocessor 7401 will also become LOW. The Front Microprocessor will also be switched off at this point.

c) Switching the unit to STANDBY via remote control or Easy Link Bus

When in **Standby** the Main Microprocessor 7335 will connect the MUTE output pin 21 to LOW.
The muting is triggered as described above.

13.3. RECOGNIZING THE TAPE-END OF A CASSETTE / QUICK REVERSE DETECTION

With the electronically controlled RED tape drive (D stands for Digital) the tape-end of a cassette is recognized in various ways by the Main Microprocessor 7335, after which the drive is switched to the following modes of operation:

a) Analog Compact Cassette (CC)

Underneath the spindles of the tape drive are the two photo-sensors 7702 and 7703. Reflectors have been mounted underneath the spindles (items 112 and 113) which, owing to their starlike shape, reflect the light from the photo-sensors differently when the spindles are in motion. As the spindles move, the photo-sensors supply rectangular pulses whose frequency depends on the rotational speed.
These rectangular pulses reach the Main Microprocessor 7335 via **DET1** and **DET2**. From the different frequencies the Main Microprocessor evaluates the following information from the **DET1** and **DET2** control signals:

- Movement of winding disks
- Position on the cassette (mathematical calculation)
- Current tape speed (search mode)
- Running time (counter)

The information regarding the calculated running time is passed to the Front Microprocessor 7401, which controls the time indication on the display. The control signal DET1 is also passed directly to the Front Microprocessor, so that the running time can also be calculated by the Front Microprocessor. Note: this facility is not used here.

Once the end of the tape is reached, the spindles stop and no further rectangular pulses are transmitted by the control lines **DET1** and **DET2**. Thus the Main Microprocessor recognizes that the end of the cassette has been reached and the tape drive is switched - depending on the operating mode – to STOP or REVERSE.

b) Blocking in the event of the tape tangling

If the spindles become blocked as a result of tape tangling in the middle of a cassette, the Main Microprocessor will recognize this in the manner as described above and immediately switch the drive to STOP. If the cassette is playing in the REPEAT mode the drive will first be switched to REVERSE. If the spindles fail to rotate after reversing direction, the drive will be switched to STOP.

c) Digital Compact Cassette (DCC)

On a cassette corresponding to the DCC standard, a reflective foil has been mounted at the end of the magnetizable part on the back of the tape.
The tape passes a photo-sensor (Tape End Sensor 1036) which is mounted on the drive. If the reflective foil now reaches the photo-sensor, the light emitted from it will be strongly reflected and the photo-sensor will deliver a HIGH level. With this control pulse the Main Microprocessor immediately switches the drive to STOP or REVERSE operation → **Quick Reverse.**

Advantage:
The tape is immediately halted at the end of the magnetizable part – the transparent start leader is not wound off.
In reverse operation the cassette will continue playing without a pause on reaching the end of the tape.
During (digital) recording hardly any of the music will be lost thanks to this **Quick Reverse** function.

The output signal of the photo-sensor (Tape End Sensor 1036) is subject to constant fluctuations because the tape reflects in a varying manner – depending on the type of tape, wrinkly patches and external influences.
For this reason the signal has to be processed before it can be delivered as a control signal to the microprocessor. This processing is performed in the **Quick Reverse Detection** circuit.
The output signal of the photo-sensor passes from the drive via plugs 1707 (RE deck electronics) and 1326 to the Main Board (QU.REV), is then rectified by D6310 (peak value rectification) and integrated by C2296. Only once the reflective foil passes the photo-sensor will the output voltage increase to the extent that D6310 is able to conduct continuously, thus fully charging C2296. The level at the inverting input of IC7308 exceeds the reference voltage created by R3195/R3196 found at the non-inverting input, and IC7308 will switch the output to LOW.
IC7308 is wired to function as a Schmitt trigger.
The Main Microprocessor 7335 now evaluates the clearly defined output in the manner as described above.

13.4. SILENCE DETECTION

The pause recognition fulfils two tasks:

1) Recognition of PAUSES on pre-recorded analog compact cassettes during rapid search (PREVIOUS and NEXT)

2) Recognition of PAUSES in the input signal. This provides the opportunity of placing a "START marker" during recording in the AUX channel.

1) Title search on pre-recorded compact cassettes

The analog signal passes from the analog playback head to the READ amplifier 7703, is amplified there and conducted via the Digital Board to the Main Board at the analog playback equalizer. After level adjustment and equalization, the composite signal LEFT + RIGHT is formed via R3335 and R3336. This composite signal is amplified by T7327 and at the same time adapted in terms of frequency (high-pass) in order to suppress low-frequency interference. In the case of DOLBY C, switch T7329 connects through R3388 as a load for the purpose of level adjustment.
The amplified composite signal passes via C2374 and C2371 to the input pin 1 of LEVEL SENSOR IC 7326.
In SEARCH, switch T7328 connects R3389 with the aid of the LEVEL control signal in order to raise the limiting frequency of the high pass by a factor of 10 to approx. 1kHz.
The composite signal is first of all amplified in IC7326 and then conducted to a comparator.
External delay elements are connected via pin 2 (Delay). This delay prevents pulse spikes and short pauses in pieces of music from resulting in erroneous switching. Switch T7330 and C2377 serve to adapt the time constant at normal speed (digital recording).
T7331 is used for inverting the LEVEL control signal.
T7324 serves for connecting C2373 to C2376 in parallel at normal speed. This increases the amplification for low frequencies.
The comparator lies with the non-inverting input at a reference voltage. The amplified and frequency-adjusted composite signal lies at the inverting input. If during pauses the composite signal drops to below the reference voltage, the comparator will switch its output to HIGH. The next drive transistor will switch through, transferring the output pin 6 to LOW = SILENCE. It is by means of this SILENCE control signal that microprocessor 7335 recognizes that a PAUSE has been found and will switch the drive from Search to Playback.

2) Digital recording on a DCC

The analog recording signal reaches the Front Board via the "Rec-in" socket, the Rec. preamplifier and plug 1302 for "rec-level" adjustment and then returns to the Main Board via plug 1302. Via Recording amplifier, relay 1307 and plug 1321 on the Digital Board it passes to the ADC. The digitized recording signal is then transmitted to the DAI.
A digital recording signal reaches the DAI directly from the digital-in socket via plug 1321.
From the DAI the digital signal is not only conducted to the digital recording branch, but also to the DAC. The signal, once again analog, travels to the Line-Out amplifier via plug 1322.
The Line-Out signal goes for monitoring:

a) at the Line-Out sockets (FIX OUT)
b) at the headphone amplifier

and for further processing

a) via plug 1425 to level display on the Front Board

b) as composite signal for SILENCE DETECTION:

The composite signal LEFT + RIGHT is created via R3379 and R3380 and is passed on via amplifier T7327 to the Level Sensor IC 7326. If a pause is recognized in the monitor signal, pin 6 will switch to LOW = SILENCE (a description of how this works is given above). Microprocessor 7335 recognizes by the SILENCE control signal that a pause has been located and will initiate a "Start Marker" on the AUX channel. In this way "Start Markers" can be incorporated in (digital) recordings.

ENGINEERS REMARKS:

FRONT BOARD (PCB4)

TRANSISTOR 7451-7456 USED AS DIODE

1400

TRACK SIDE A B TOTAL REM TIME WRITE MARK ERASE CC dcc

TRACK REPEAT CONT L DOLBY B C NR

DIGITAL ANALOGUE_dB 60 50 40 30 25 20 15 12 9 6 4 2 0 RECORD

F2 FROM 1425/16 — 2435 100N — 2436 100N

F1 FROM 1425/14 — 2437 100N

3.9V ~

7403 BC847B — 3418 68K — 3416 10K — -30V

7402 BC847B — 3417 68K — 3415 10K — -30V

I/O PORT 7 | I/O PORT 8 | I/O PORT 9 | I/O PORT 6 | I/O PORT 4 | I/O PORT 0 | I/O PORT 5 | I/O PORT 3 | I/O PORT 1

DATA MEMORY (RAM) 512X8 BIT

PROGR MEMORY (ROM) 24KX8 BIT

PROGRAM COUNTER

C P U

16 BIT TIMER/COUNTER | INTERRUPT CONTROLLER | 8 BIT TIMER/COUNTER

7401 TMP87CK70F

CLOCK/TIMING CONTROLLER (I/O PORT 2)

6 BIT A/D CONVERTER

4.194MHz

+5V | -30V | VDD | VKK | CSSS IN2 | STBY | EL SW | RESET | TEST

DOLBY C | MTS | DATA | CLOCK | IR-EYE | DOLBY OFF | DET1 | L OUT | SRES | CSSS INT | CSSS IND | ER PR | HOLE 3 | HOLE 4 | HOLE 5 | IR-EYE | EL IN | HRES | EL OUT

3458 10K | 3459 10K | 3400 10K

3455 10K | 3454 10K | 3453 10K | 3452 10K | 3451 10K | 3413 10K

3419 47K — 2439 4MU

FROM 142S +TRAY — CURRENT PATH DURING "TRAY OUT"

7406 BC807/40 — 3447 330 — 3445 330

7405 BC807/40 — 3446 330 — 3444 330

7416 BC848 — 7408 BC817/40 — 6421 BAS16

7407 BC817/40 — 6422 BAS16 — 7414 BC848

3449 3K3 — 3448 3K3

5410 15MUH — 2431 47MU — 2432 100N — 3443 10K

TRAY IN=HIGH

TRAY OUT=HIGH

OUT=LOW — IN=LOW

1423: GND | MOT- | MOT+ | TRAY OUT | TRAY IN | S

TRAY MOTOR

TO/FROM 143S (TRAY IND BOARD)

3457 10K — 3456 10K

IR-EYE — 7410 GP1U 500X — 2455 100N — GND — +MUP — IR IN — 3464 100 — 42 — IR-EYE TO 7401 PIN 3. 18

2449 47MU

3465 10K X

L=PROTECTED | H=DCC L=CC

TO/FROM 1601 (DCC INDICATOR BOARD) 1402: COM A | COM B | CASS IND | HOLE3 | HOLE4 | HOLE5 | +10V | QU REV | ER PR | GND | CASS IND | L11

TO 2442 | TO 2441

1425: IN | GND | L IN | +12V | QU.REV | -12V | COM B | COM A | +5V | STBY | GND | ELSW | F2 | CLOCK | F1 | MTS | -30V | EL IN | EL OUT | DOLBY C | CASS IND | +TRAY | S REC | HOLDT OFF | H RES | DET 1 | DATA | GND

2453 100N — 2452 100N — 2451 10N

TO 7405

TO/FROM 1326 (MAIN BOARD)

Δ ...FOR DCC300 ONLY

X ...FOR DCC380 ONLY

7451 BC848 — 7452 BC848 — 7453 BC848 — 7454 BC848 — 7455 BC848 — 7456 BC848

1406 APPEND | 1415 PREV | 1404 STOP | 1413 MRK.WRITE | 1401 OPEN | 1412 REWIND

1407 RECORD | 1414 NEXT | 1402 PLAY | 1417 MRK.ERASE | 1416 FORWARD | 1409 ANA/DIG

1403 PAUSE | 1408 REC.MUTE | 1405 DOLBY OFF/B/C

1418 MODE | 1410 TIME TEXT

1411 COUNTER RESET

1424: LED | +UP | GND | KSTR | BRCK | A/B | REPEAT

TO/FROM 1430 (KEYBOARD)

RECORDING LEVEL CONTROL

1426: +12 | L1 | L2 | GND A | GNDR | R2 | R1 | -12

10.9V — 2481 10N — 3312 50K — 3467 2K2 — 3471 15K — 1/2 7471 7.0V NJM5532MD — 3473 10 — 2475 560P — 3470 1K — 3474 10 — 3468 2K2 — 3472 15K — 2482 10N

REC LEVEL LEFT — REC LEVEL RIGHT

TO/FROM 1302 (MAIN BOARD)

PEAK LEVEL DETECTION

7467 BC848B — 7465 BC848B — 7468 BC848B — 7466 BC848B

1/2 7412 NJM4560M — 1/2 7411 NJM4560M — 1/2 7413 NJM4560M

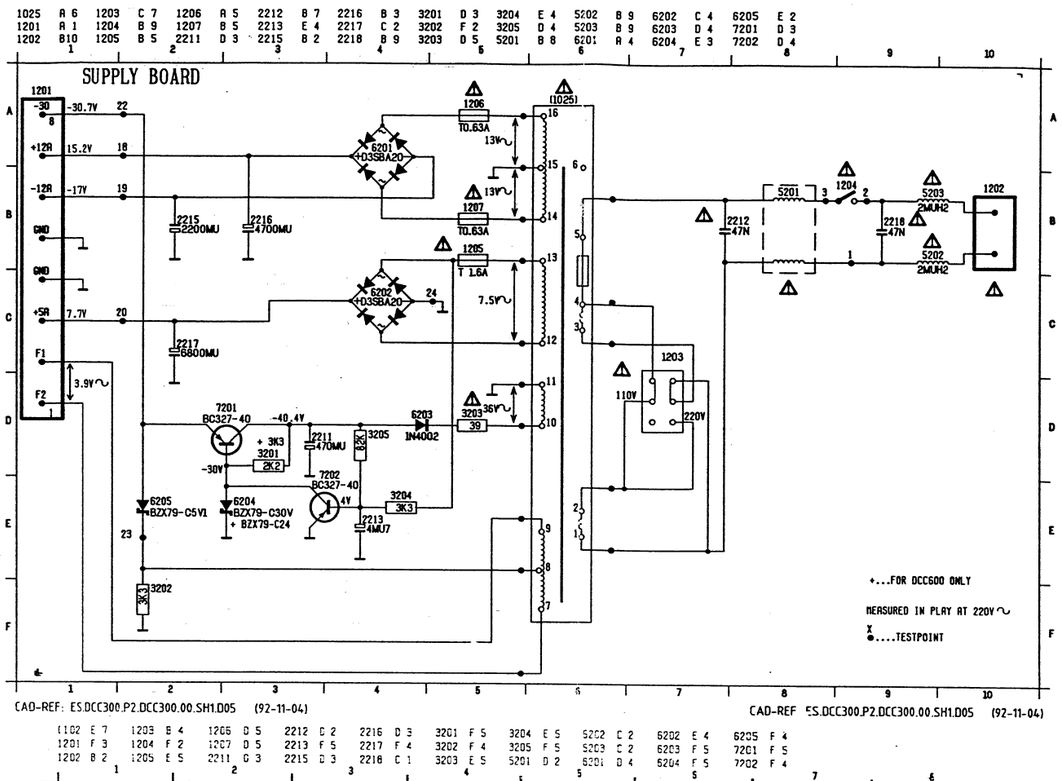
LEFT HIGH-LEVEL 0 → -30dB — LEFT LOW-LEVEL -30 → -60dB

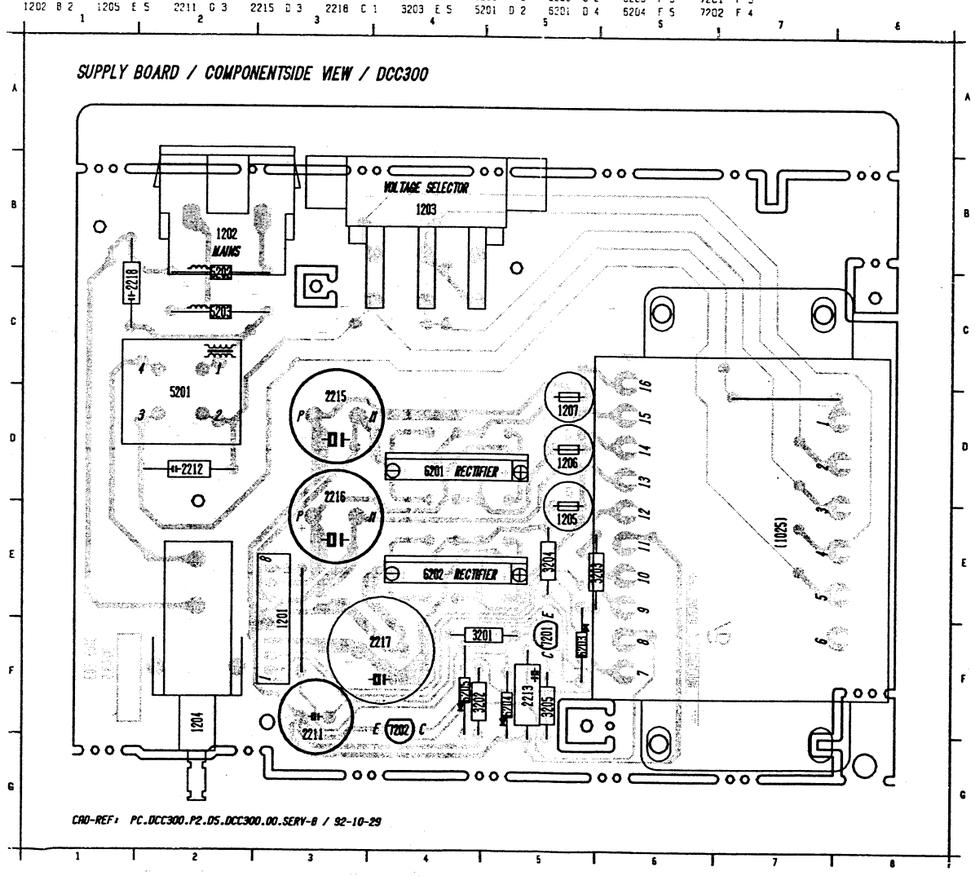
RIGHT HIGH-LEVEL 0 → -30dB — RIGHT LOW-LEVEL -30 → -60dB

FROM 1425 L IN — FROM 1425 R IN

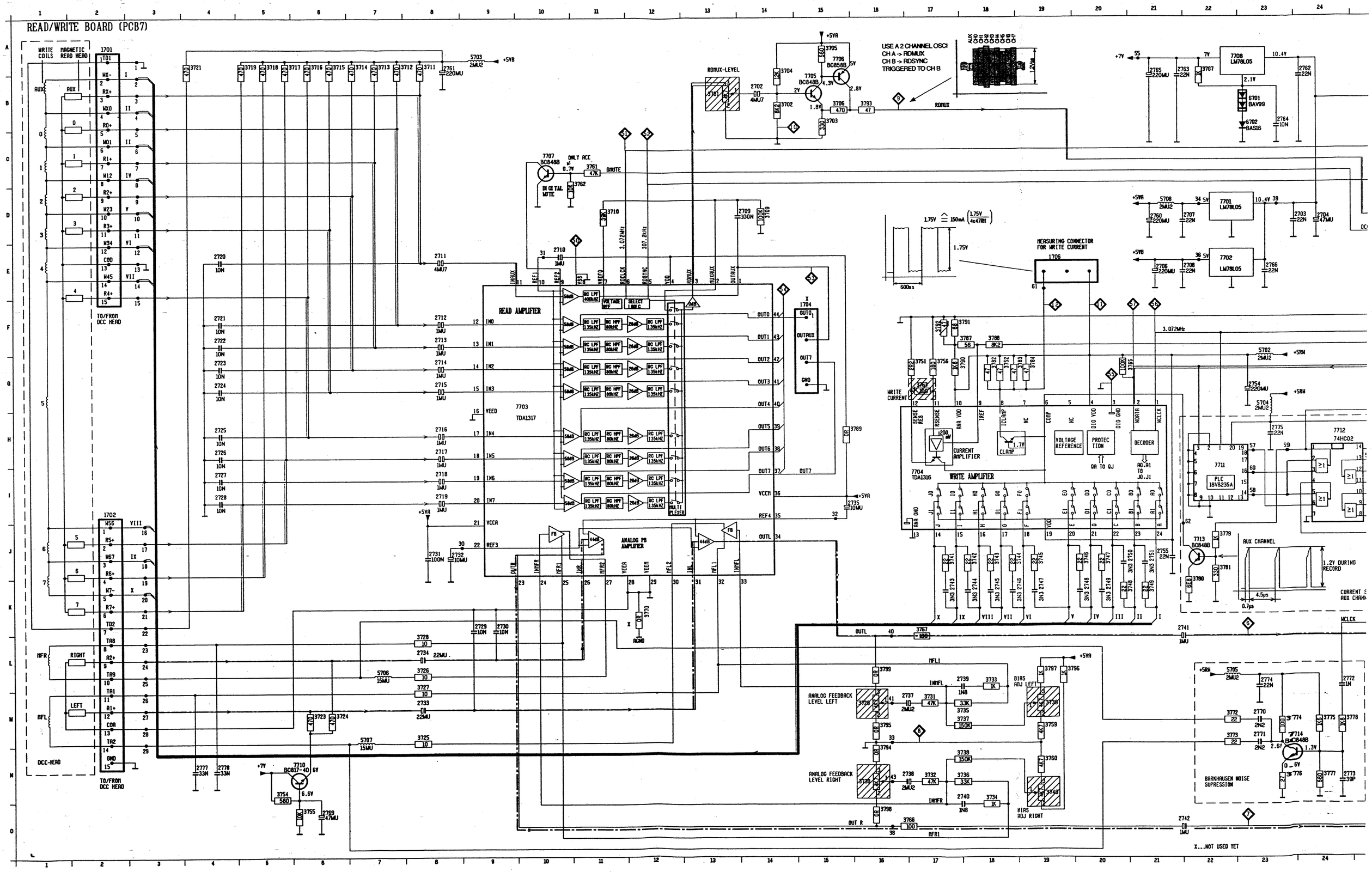
VOLTAGES ON SEMICONDUCTORS DEPEND ON INPUT SIGNAL

CAD-REF: ES.DCC300.P4.DCC300.00.SH1.D05 (92-10-29)


1025 A 6 1203 C 7 1206 A 5 2212 B 7 2216 B 3 3201 D 3 3204 E 4 5202 B 9 6202 C 4 6205 E 2
1201 A 1 1204 B 9 1207 B 5 2213 E 4 2217 C 2 3202 F 2 3205 D 4 5203 B 9 6203 D 4 7201 D 3
1202 B10 1205 B 5 2211 D 3 2215 B 2 2218 B 9 3203 D 5 5201 B 8 6201 A 4 6204 E 3 7202 D 4
SUPPLY BOARD
1201
-30
-12R
GND
GND
+5R
F1
F2
-30.7V
15.2V
-17V
7.7V
3.9V
22
18
19
20
23
2215 2200MU
2216 4700MU
2217 6800MU
6201 D3SBA20
6202 D3SBA20
24
1206 T0.63A
1207 T0.63A
1205 T 1.6A
13V
13V
7.5V
3203 39
36V
7201 BC327-40
-40.4V
+ 3K3
3201 2K2
-30V
2211 470MU
3205 2K2
6203 1N4002
7202 BC327-40
4V
3204 3K3
2213 4MJ7
6205 BZX79-C5V1
6204 BZX79-C30V
+ BZX79-C24
3202 3K3
(1025)
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
5201
1204
2212 47N
2218 47N
5203 2MUH2
5202 2MUH2
1202
1203
110V
220V
+...FOR DCC600 ONLY
MEASURED IN PLAY AT 220V~
X ....TESTPOINT
CAD-REF: ES.DCC300.P2.DCC300.00.SH1.D05 (92-11-04)
CAD-REF ES.DCC300.P2.DCC300.00.SH1.D05 (92-11-04)


E 7 1203 B 4 1206 D 5 2212 D 2 2216 D 3 3201 F 5 3204 E 5 5202 C 2 6202 E 4 6205 F 4
F 3 1204 F 2 1207 D 5 2213 F 5 2217 F 4 3202 F 4 3205 F 5 5203 C 2 6203 F 5 7201 F 5
B 2 1205 E 5 2211 G 3 2215 D 3 2218 C 1 3203 E 5 5201 D 2 6201 D 4 6204 F 5 7202 F 4
SUPPLY BOARD / COMPONENTSIDE VIEW / DCC300
VOLTAGE SELECTOR
1203
1202
MAINS
5202
5203
+I- 2218
5201
+I- 2212
2215
2216
2217
2211
1201
1204
6201 RECTIFIER
6202 RECTIFIER
1207
1206
1205
3204
3203
3201
C 7201 E
C 7202 E
3202
2213
3205
(1025)
CAD-REF: PC.DCC300.P2.D5.DCC300.00.SERV-B / 92-10-29

READ/WRITE BOARD (PCB7)



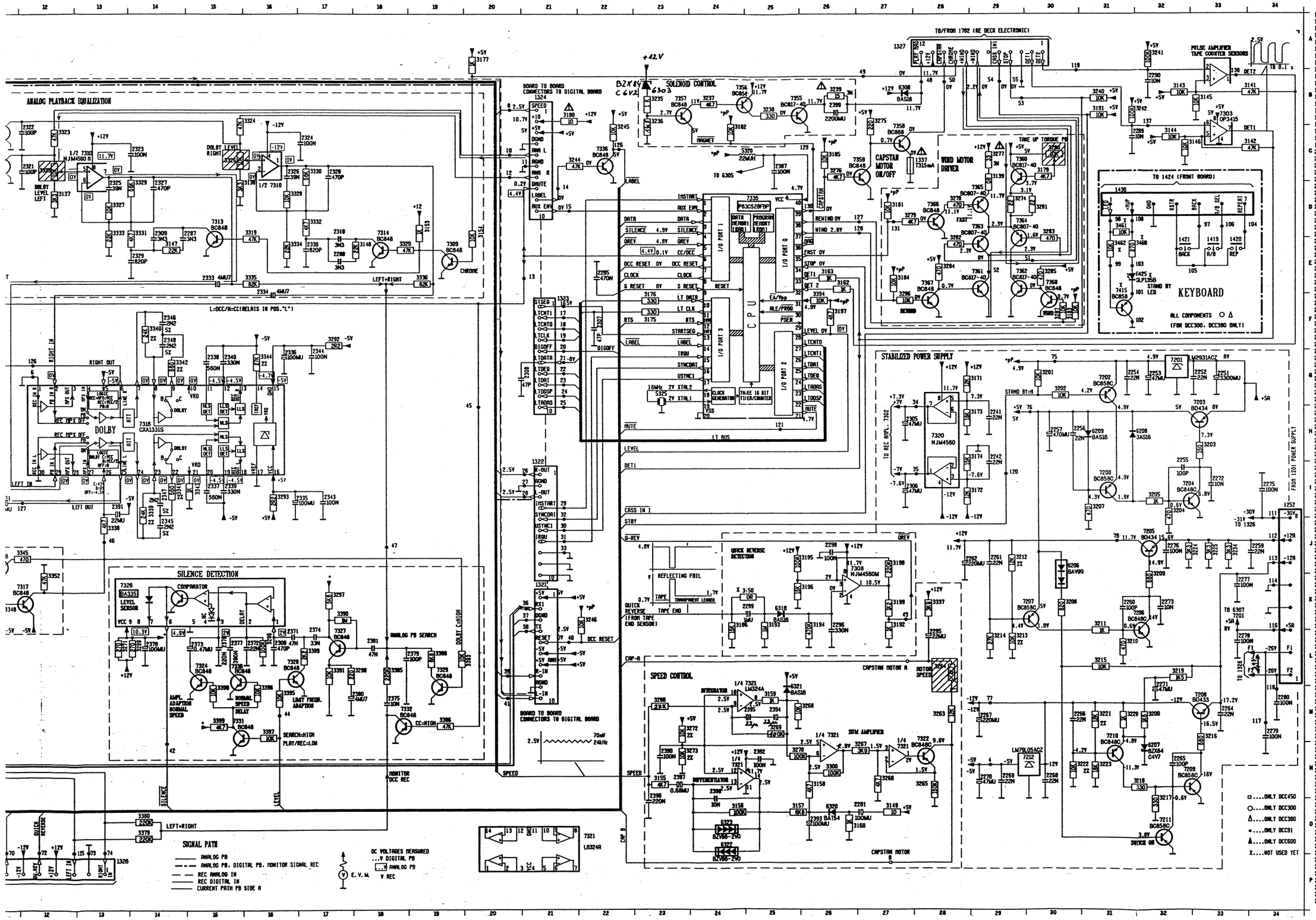
CAD-REF: ES.DCC300.P7.DCC300.00.SH1.D06 (92-11-11)

MAIN BOARD (PCB3)

1701	A 2	3752	G18	2741	I 4	3803	K 9
1702	I 2	3754	N 5	2742	I 4	3804	K 9
1704	F15	3755	G 6	2743	I 4	3805	K 9
1705	B27	3756	G17	2744	I 4	3806	K 9
1706	E19	3759	M19	2745	I 4	3807	K 9
1708	K26	3760	N19	2746	I 4	3808	K 9
2702	B14	3761	C11	2747	I 4	3809	K 9
2703	D23	3762	C10	2748	I 4	3810	K 9
2704	D24	3763	G17	2749	I 4	3811	K 9
2706	E21	3765	G21	2750	I 4	3812	K 9
2707	D21	3766	D17	2751	I 4	3813	K 9
2708	E21	3767	L17	2752	I 4	3814	K 9
2709	D13	3770	K12	2753	I 4	3815	K 9
2710	E10	3772	M22	2754	I 4	3816	K 9
2711	E 8	3773	M22	2755	I 4	3817	K 9
2712	F 8	3774	M23	2756	I 4	3818	K 9
2713	F 8	3775	M24	2757	I 4	3819	K 9
2714	G 8	3776	N23	2758	I 4	3820	K 9
2715	G 8	3777	N24	2759	I 4	3821	K 9
2716	H 8	3778	M24	2760	I 4	3822	K 9
2717	H 8	3779	J22	2761	I 4	3823	K 9
2718	I 8	3780	N22	2762	I 4	3824	K 9
2719	I 8	3781	J22	2763	I 4	3825	K 9
2720	E 4	3782	G18	2764	I 4	3826	K 9
2721	F 4	3783	G19	2765	I 4	3827	K 9
2722	F 4	3784	G19	2766	I 4	3828	K 9
2723	G 4	3787	F18	2767	I 4	3829	K 9
2724	G 4	3788	F18	2768	I 4	3830	K 9
2725	H 4	3789	H15	2769	I 4	3831	K 9
2726	H 4	3790	G18	2770	I 4	3832	K 9
2727	I 4	3791	F17	2771	I 4	3833	K 9
2728	I 4	3792	F17	2772	I 4	3834	K 9
2729	K 9	3793	B16	2773	I 4	3835	K 9
2730	K 9	3794	M16	2774	I 4	3836	K 9
2731	J 8	3795	L16	2775	I 4	3837	K 9
2732	J 8	3796	L19	2776	I 4	3838	K 9
2733	M 8	3797	L19	2777	I 4	3839	K 9
2734	L 8	3798	D16	2778	I 4	3840	K 9
2735	I15	3799	L16	2779	I 4	3841	K 9
2737	M17	5701	B25	2780	I 4	3842	K 9
2738	N17	5702	F23	2781	I 4	3843	K 9
2739	L18	5703	A 9	2782	I 4	3844	K 9
2740	N18	5704	G23	3701	B13	3845	K 9
2741	K22	5705	L22	3702	B14	3846	K 9
2742	O22	5706	L 7	3703	B15	3847	K 9
2743	K17	5707	M 7	3704	A14	3848	K 9
2744	K18	5708	D21	3705	A15	3849	K 9
2745	K18	6701	B23	3706	B15	3850	K 9
2746	K19	6702	B23	3707	A22	3851	K 9
2747	K19	7701	D22	3709	D14	3852	K 9
2748	K20	7702	E22	3710	D11	3853	K 9
2749	K20	7703	G 9	3711	A 8	3854	K 9
2750	J21	7704	I16	3712	A 7	3855	K 9
2751	J21	7705	B15	3713	A 7	3856	K 9
2754	O23	7706	A15	3714	A 7	3857	K 9
2755	J21	7707	C10	3715	A 6	3858	K 9
2760	D21	7708	A22	3716	A 6	3859	K 9
2761	A 8	7710	N 6	3717	A 5	3860	K 9
2762	A24	7711	I22	3718	A 5	3861	K 9
2763	A21	7712	H24	3719	A 5	3862	K 9
2764	B23	7713	J22	3721	A 4	3863	K 9
2765	A21	7714	M24	3723	M 6	3864	K 9
2766	E23			3724	M 6	3865	K 9
2769	O 6			3725	M 8	3866	K 9
2772	N23			3726	L 8	3867	K 9
2771	N23			3727	L 8	3868	K 9
2772	L24			3728	L 8	3869	K 9
2773	N24			3729	M16	3870	K 9
2774	L23			3730	N16	3871	K 9
2775	H23			3731	M17	3872	K 9
2776	E25			3732	N17	3873	K 9
2777	N 4			3733	L18	3874	K 9
2778	N 4			3734	N18	3875	K 9
2781	E26			3735	M18	3876	K 9
2782	E26			3736	N18	3877	K 9
				3737	M18	3878	K 9
				3738	N18	3879	K 9
				3739	N19	3880	K 9
				3740	N19	3881	K 9
				3741	J17	3882	K 9
				3742	J18	3883	K 9
				3743	J18	3884	K 9
				3744	J19	3885	K 9
				3745	J19	3886	K 9
				3746	J20	3887	K 9
				3747	J20	3888	K 9
				3748	K21	3889	K 9
				3749	K21	3890	K 9
				3751	G17		

X...NOT USED YET

CAD-REF: ES.DCC300.P3.DCC300.00.SH1.D05 (92-10-30)



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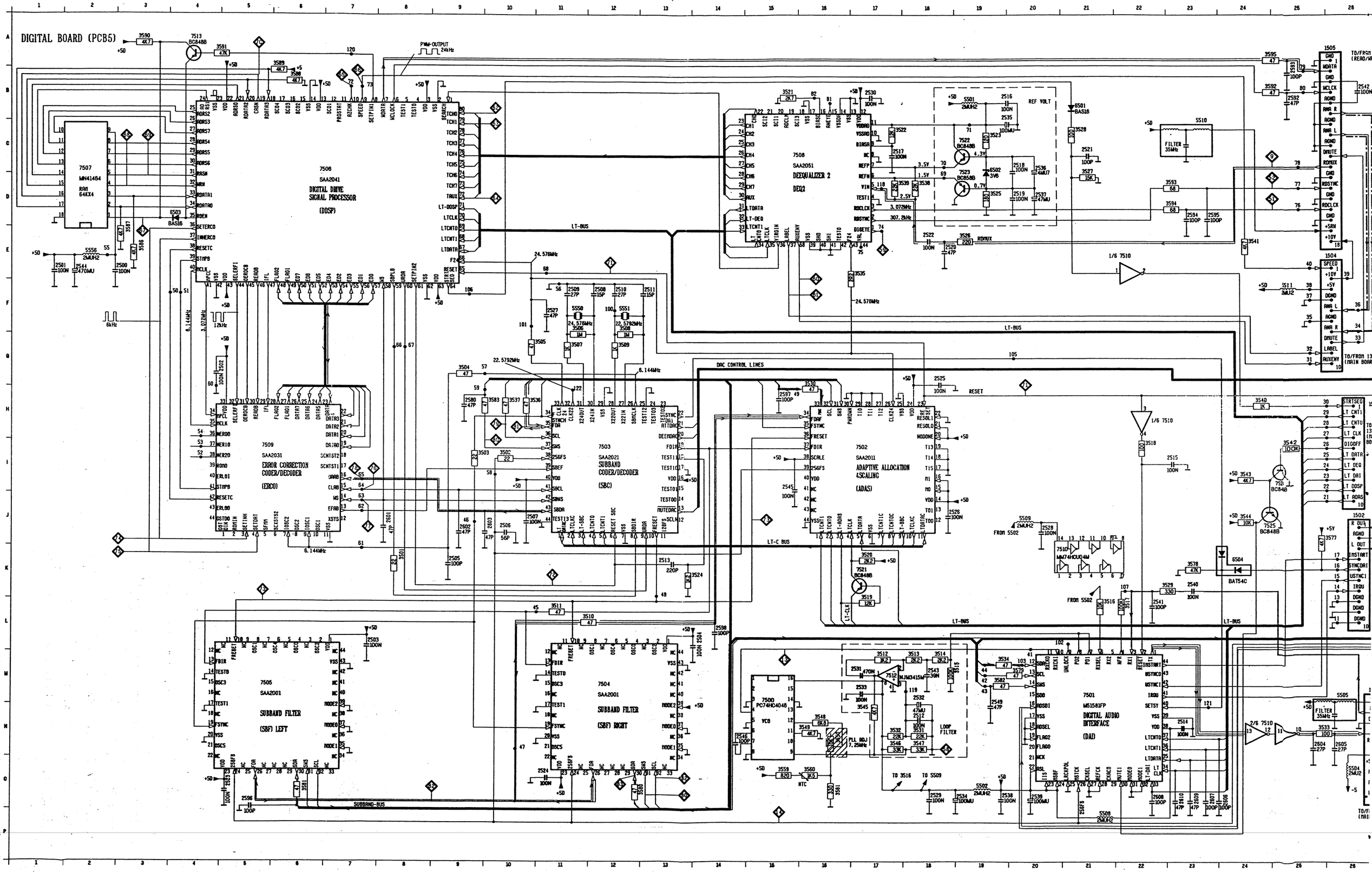
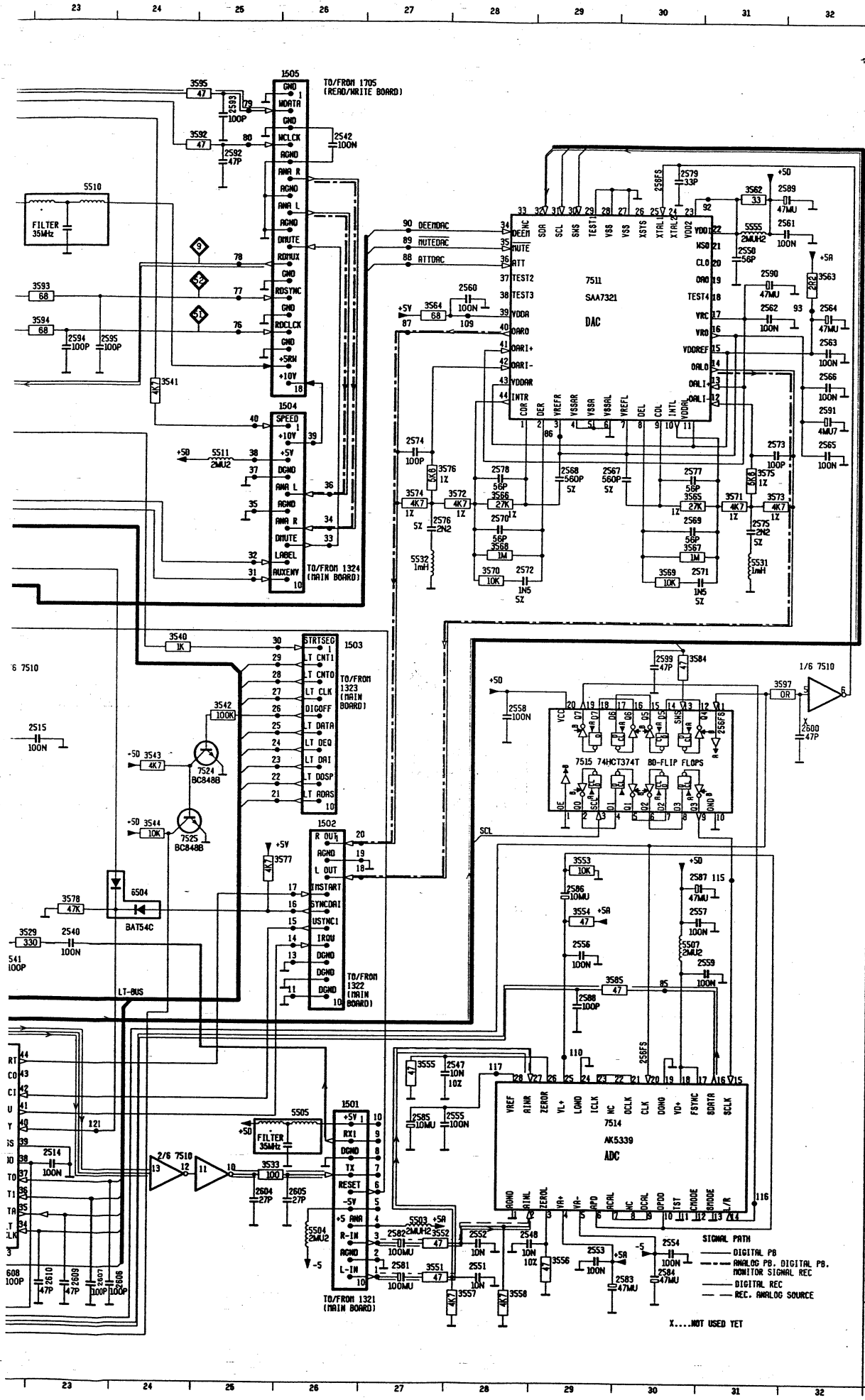
DIGITAL BOARD (PCB5)





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